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(12) United States Patent
Yoshida

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(54) DISPLAY DEVICE

(71) Applicant: **Semiconductor Energy Laboratory Co., Ltd.**, Atsugi-shi, Kanagawa-ken (JP)

(72) Inventor: **Yasunori Yoshida**, Kanagawa (JP)

(73) Assignee: **Semiconductor Energy Laboratory Co., Ltd.**, Atsugi-shi, Kanagawa-ken (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **14/170,693**

(22) Filed: **Feb. 3, 2014**

(65) **Prior Publication Data**

US 2014/0176405 A1 Jun. 26, 2014

Related U.S. Application Data

(63) Continuation of application No. 11/972,159, filed on Jan. 10, 2008, now Pat. No. 8,643,583.

(30) **Foreign Application Priority Data**

Jan. 12, 2007 (JP) 2007-004106

(51) **Int. Cl.**
G09G 3/36 (2006.01)
G09G 3/20 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***G09G 3/2085*** (2013.01); ***G09G 3/20*** (2013.01); *G02F 1/136213* (2013.01); *G09G 3/3208* (2013.01); *G09G 3/342* (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC G09G 3/20; G09G 3/2085; G09G 3/342; G09G 3/3648; G09G 2310/04; G09G 2320/0252
USPC 345/84, 89, 98, 10, 102
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,828,367 A 10/1998 Kuga
5,978,052 A 11/1999 Ilcisin
(Continued)

FOREIGN PATENT DOCUMENTS

EP 1 596 353 A2 11/2005
EP 1662469 A 5/2006
(Continued)

OTHER PUBLICATIONS

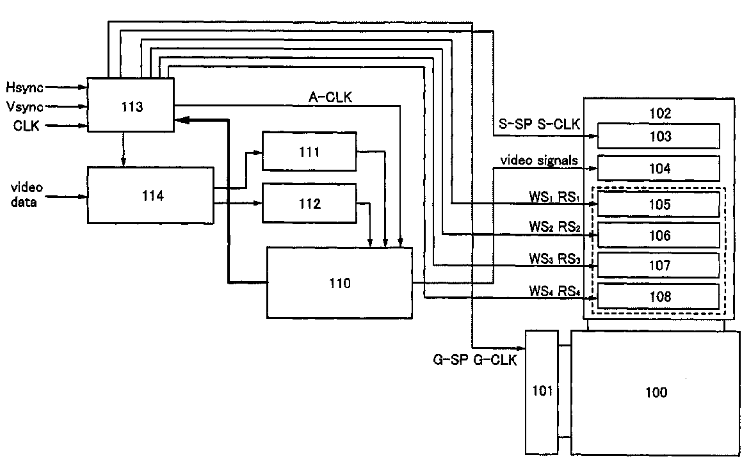
Korean Office Action (Application No. 2008-0003371) Dated Jul. 30, 2014.

Primary Examiner — Premal Patel
(74) *Attorney, Agent, or Firm* — Fish & Richardson P.C.

(57) **ABSTRACT**

To provide an active matrix display device in which power consumption of a signal line driver circuit can be suppressed, so that power consumption of the entire memory can be suppressed. A plurality of memory circuits which can write data of a video signal input to a pixel in one line period and can hold the data are provided in a signal line driver circuit of a display device. Then, the data held in each memory circuit is input to a pixel of a corresponding line as a video signal. By providing two or more memory circuits in a driver circuit, pieces of data of video signals corresponding to two or more line periods can be concurrently held in the memory circuits.

13 Claims, 87 Drawing Sheets



(51) **Int. Cl.**
G02F 1/1362 (2006.01)
G09G 3/32 (2006.01)
G09G 3/34 (2006.01)

(52) **U.S. Cl.**
CPC *G09G 3/3648* (2013.01); *G09G 2310/024* (2013.01); *G09G 2310/027* (2013.01); *G09G 2310/04* (2013.01); *G09G 2310/061* (2013.01); *G09G 2320/0252* (2013.01); *G09G 2330/021* (2013.01); *G09G 2340/16* (2013.01)

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,054,974	A	4/2000	Sakai et al.	
6,392,619	B1	5/2002	Nitta	
6,683,596	B2	1/2004	Ozawa	
6,724,377	B2	4/2004	Ouchi	
6,750,835	B2	6/2004	Azami	
6,885,385	B2	4/2005	Ouchi	
7,110,009	B2	9/2006	Ooishi	
7,119,782	B2	10/2006	Sunohara	
7,123,227	B2	10/2006	Azami	
7,184,016	B2	2/2007	Bu et al.	
7,382,345	B2	6/2008	Hong	
7,586,485	B2	9/2009	Teshirogi	
7,710,375	B2	5/2010	Azami	
8,446,353	B2	5/2013	Azami	
2004/0125067	A1	7/2004	Kim et al.	
2005/0041488	A1	2/2005	Ito	
2005/0134189	A1*	6/2005	Osame et al.	315/169.1
2005/0134546	A1	6/2005	Woo	
2006/0020918	A1	1/2006	Mosberger	
2006/0071892	A1	4/2006	Sakaguchi	
2006/0109229	A1	5/2006	Iwabuchi	
2006/0124897	A1	6/2006	Shingai et al.	
2006/0202918	A1	9/2006	Kim	
2006/0208997	A1	9/2006	Sunohara	
2006/0255855	A1	11/2006	Nakao	
2006/0262076	A1	11/2006	Kawasaki	
2007/0008252	A1	1/2007	Seki	
2007/0109431	A1	5/2007	Lee	
2007/0252798	A1	11/2007	Wu	
2013/0100094	A1	4/2013	Shingai et al.	
2013/0249890	A1	9/2013	Azami	

FOREIGN PATENT DOCUMENTS

EP	1701329	A	9/2006
JP	04-110994	A	4/1992
JP	05-297827	A	11/1993
JP	09-159993	A	6/1997
JP	10-020809	A	1/1998
JP	11-095729	A	4/1999
JP	11-327712	A	11/1999
JP	2000-194305	A	7/2000
JP	2000-227608	A	8/2000
JP	2001-249650	A	9/2001
JP	2001-306014	A	11/2001
JP	2002-215092	A	7/2002
JP	2002-297094	A	10/2002
JP	3338259	A	10/2002
JP	2003-323147	A	11/2003
JP	2004-246325	A	9/2004
JP	3593392	A	11/2004
JP	2005-173618	A	6/2005
JP	2005-326633	A	11/2005
JP	2006-251799	A	9/2006
JP	2007-017647	A	1/2007
KR	2005-0012159	A	1/2005
KR	2006-0098135	A	9/2006
WO	WO-2005/024774		3/2005

* cited by examiner

FIG. 1

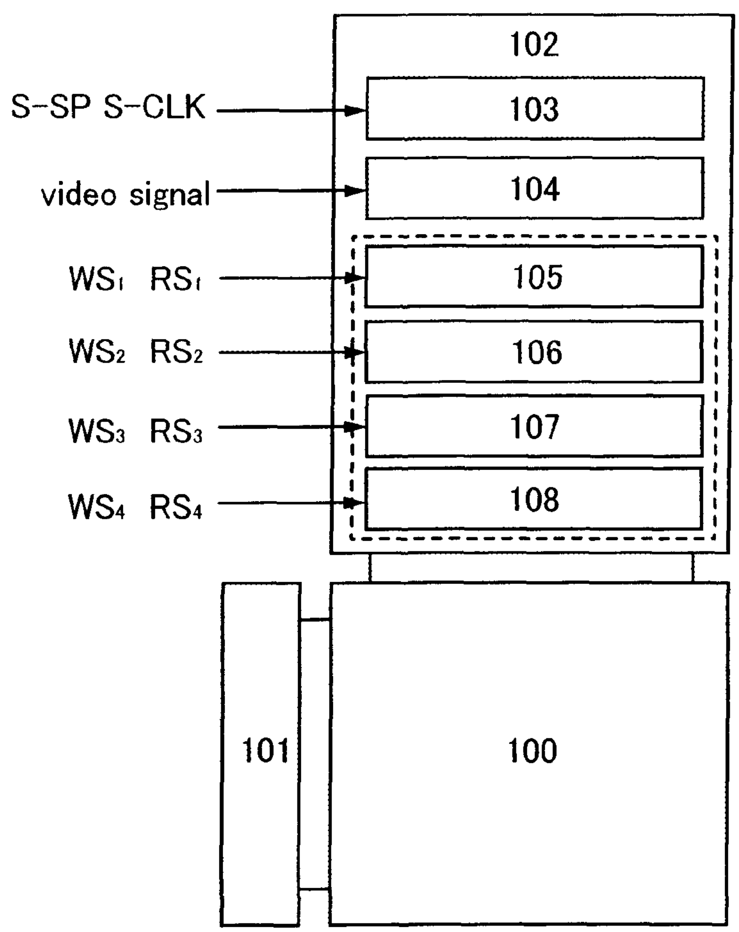

102
S-SP S-CLK
103
video signal
104
WS1 RS1
105
WS2 RS2
106
WS3 RS3
107
WS4 RS4
108
101
100

FIG. 2A

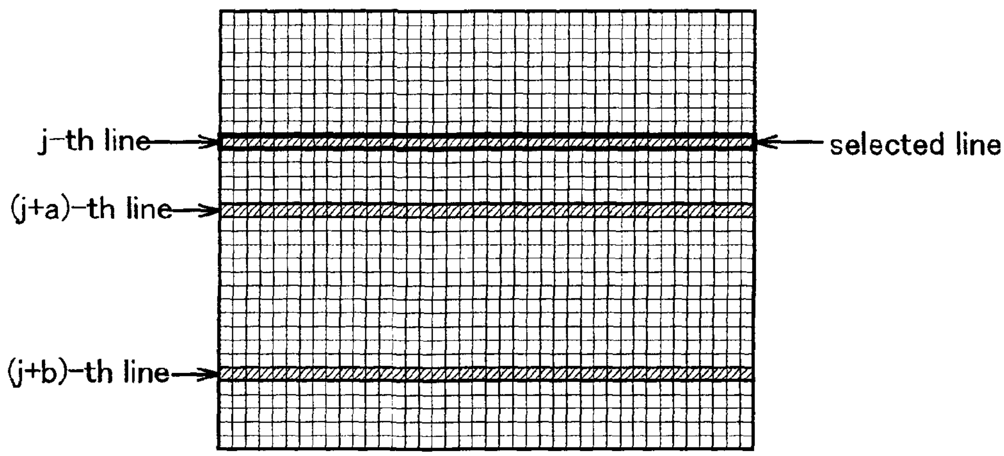

j-th line
selected line
(j+a)-th line
(j+b)-th line

FIG. 2B

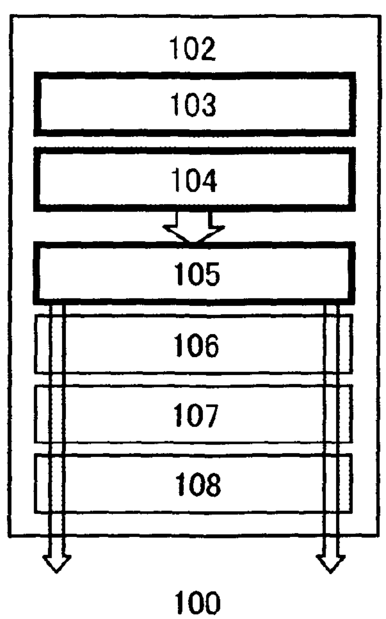

102
103
104
105
106
107
108
100

FIG. 3A

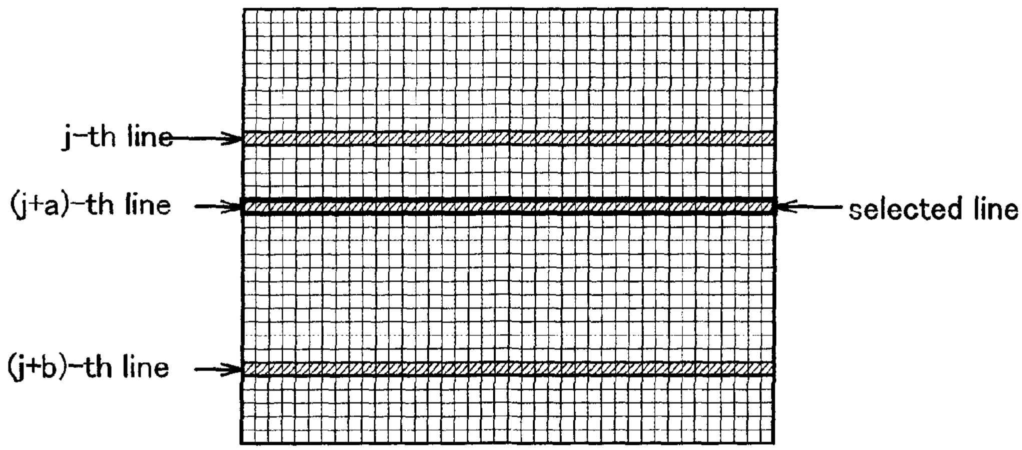

j-th line
(j+a)-th line
(j+b)-th line
selected line

FIG. 3B

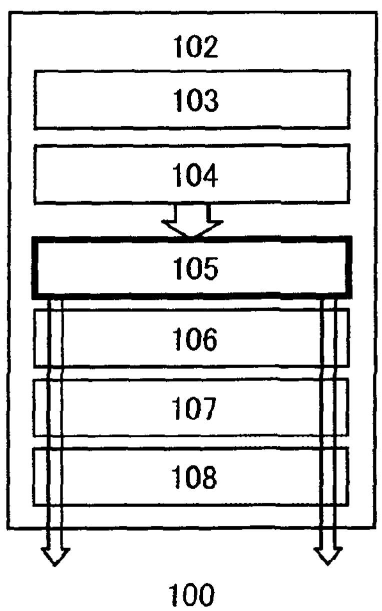

102
103
104
105
106
107
108
100

FIG. 4A

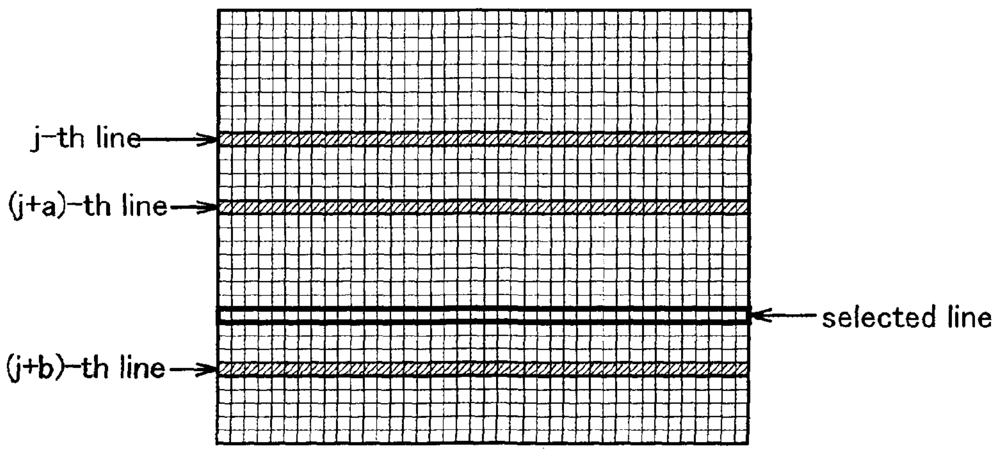

j-th line
(j+a)-th line
selected line
(j+b)-th line

FIG. 4B

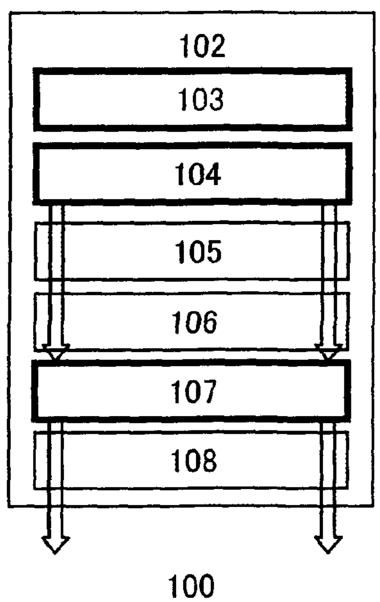

102
103
104
105
106
107
108
100

FIG. 5

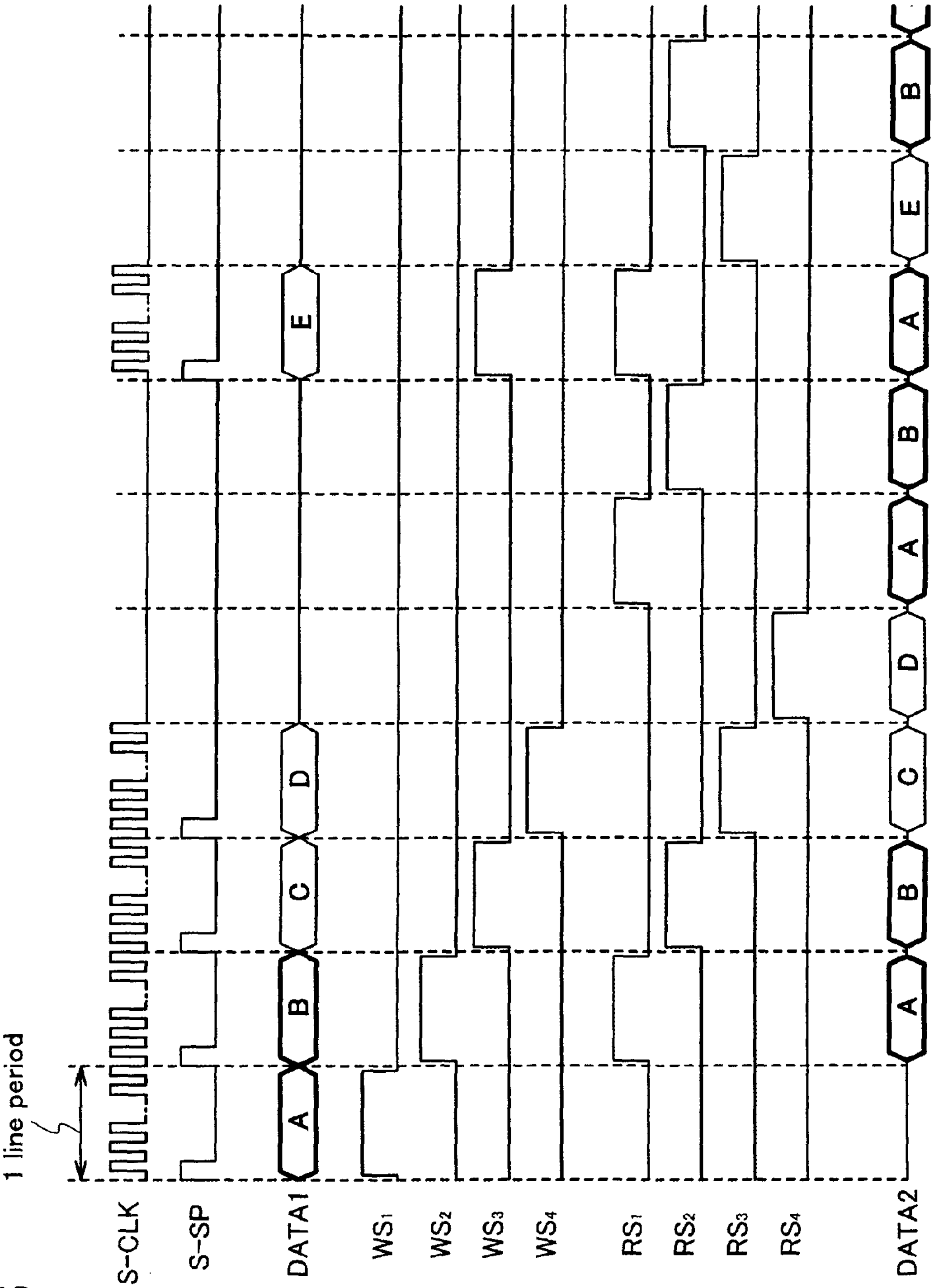
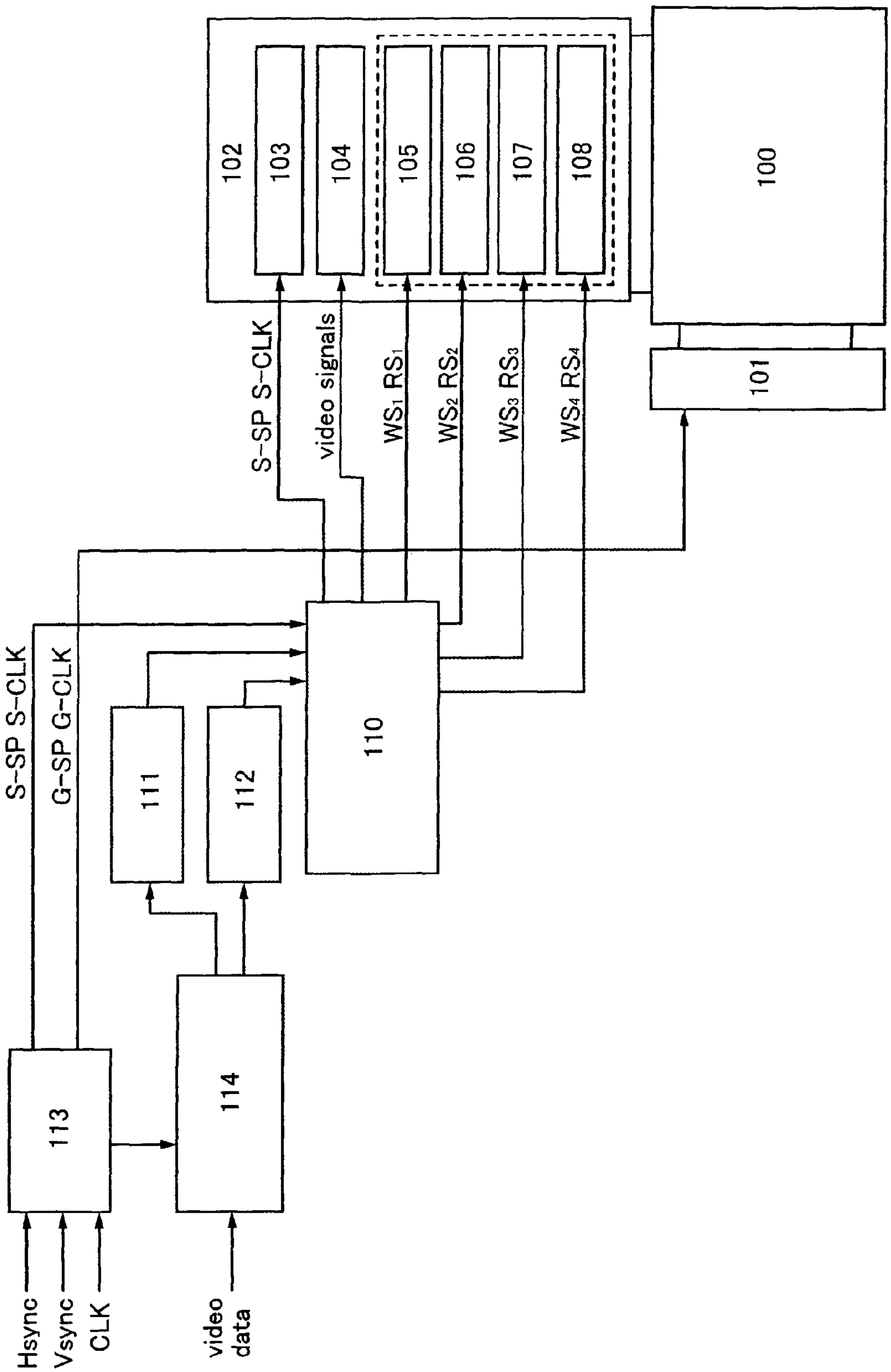

1 line period
S-CLK
S-SP
DATA1
WS1
WS2
WS3
WS4
RS1
RS2
RS3
RS4
DATA2
A
B
C
D
E

FIG. 6



102
103
104
105
106
107
108
100
101
S-SP S-CLK
video signals
WS₁ RS₁
WS₂ RS₂
WS₃ RS₃
WS₄ RS₄
S-SP S-CLK
G-SP G-CLK
111
112
110
113
114
Hsync
Vsync
CLK
video
data

FIG. 7

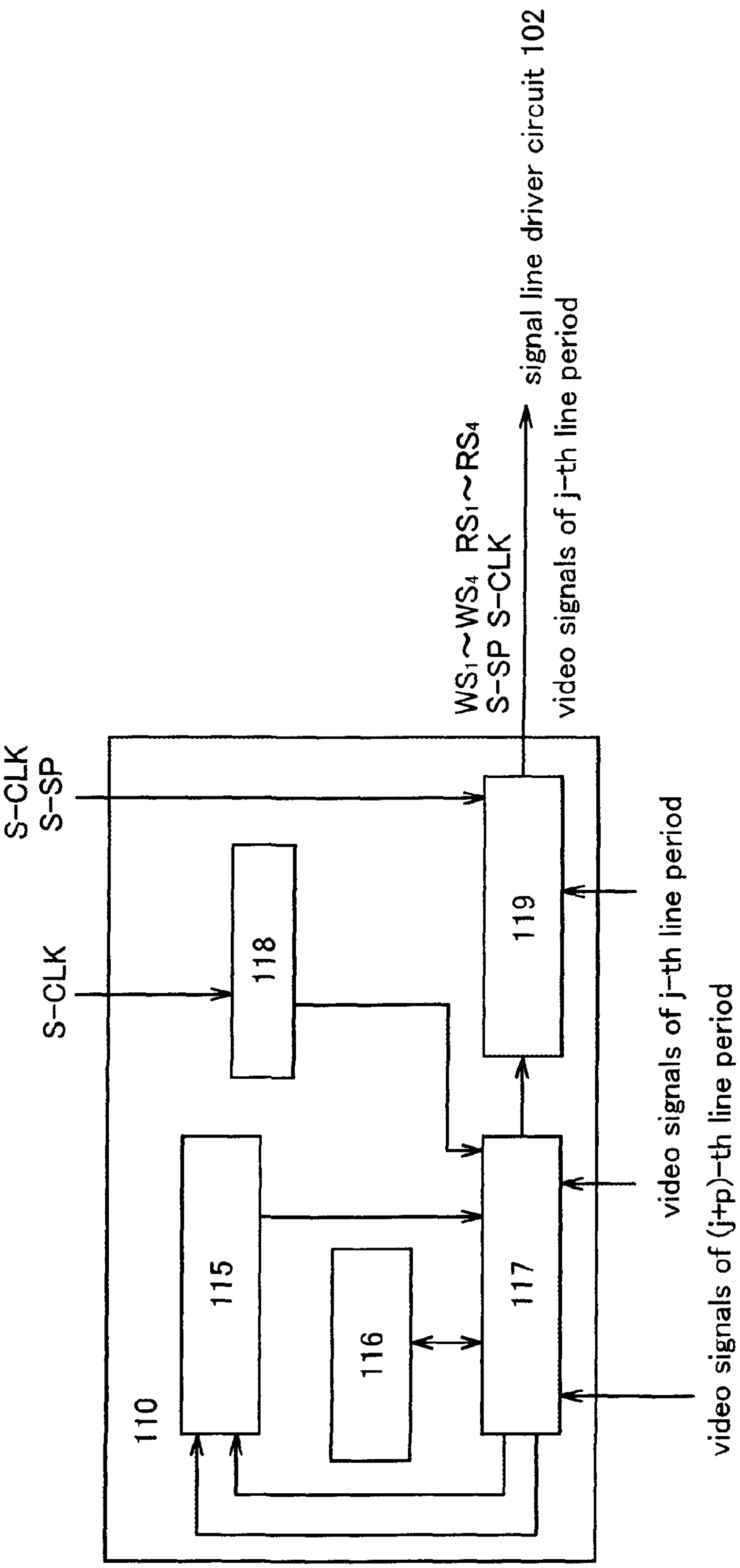
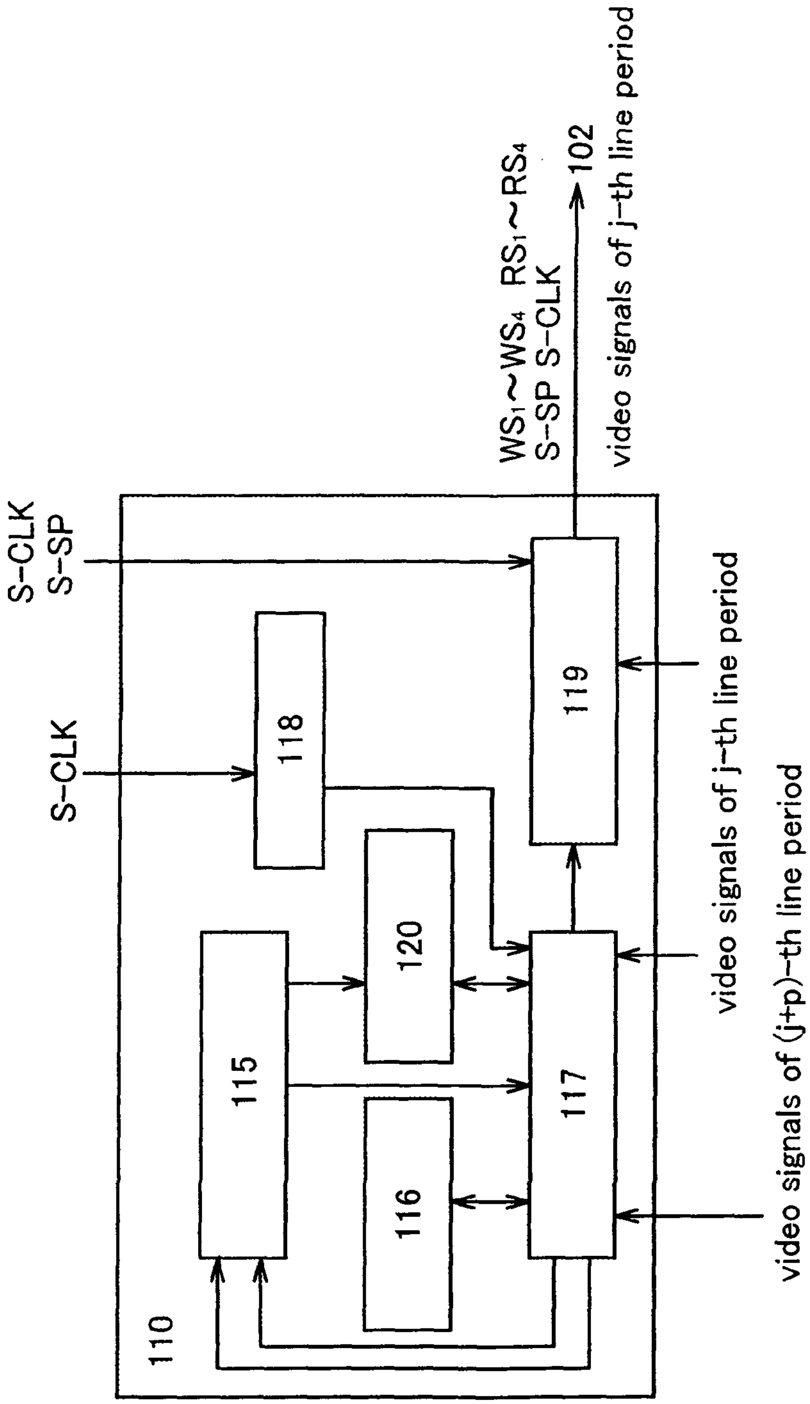
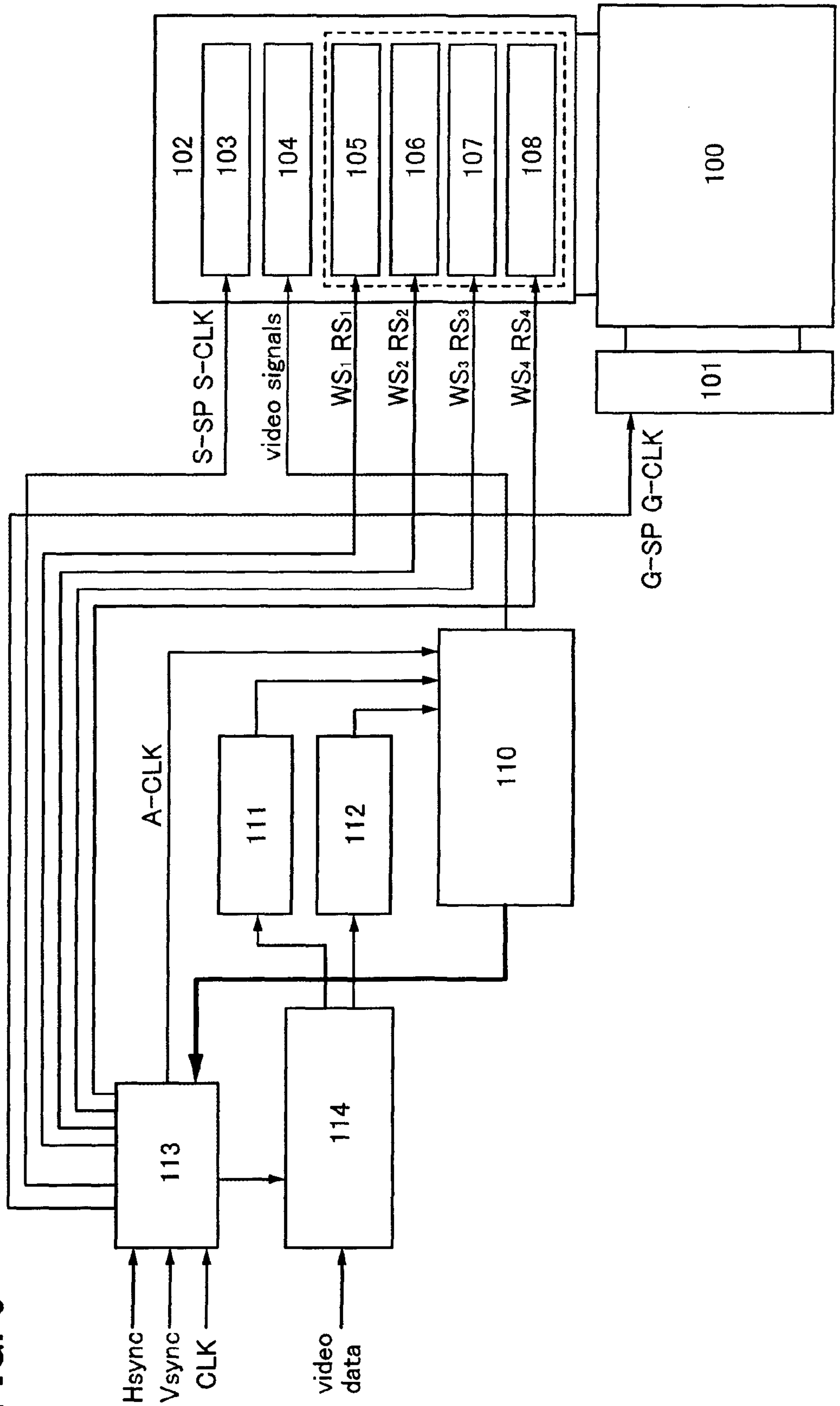

signal line driver circuit 102
WS1~WS4 RS1~RS4
S-SP S-CLK
video signals of j-th line period
S-CLK
S-SP
S-CLK
110
115
116
117
118
119
video signals of j-th line period
video signals of (j+p)-th line period
video signals of j-th line period

FIG. 8



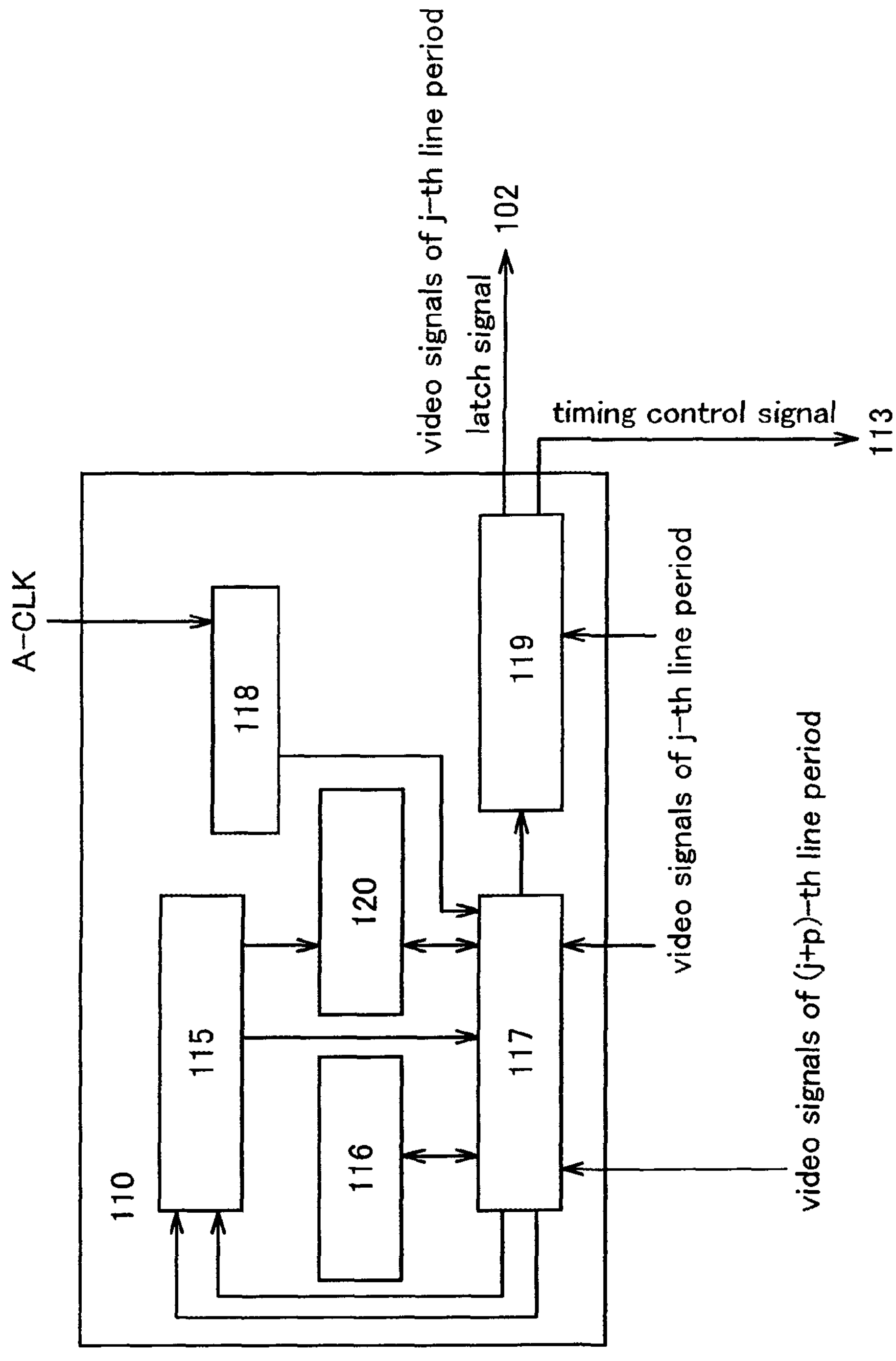
110
115
116
117
118
119
120
S-CLK
S-CLK
S-SP
WS_1～WS_4 RS_1～RS_4
S-SP S-CLK
102
video signals of j-th line period
video signals of j-th line period
video signals of (j+p)-th line period
video signals of (j+p)-th line period

FIG. 9



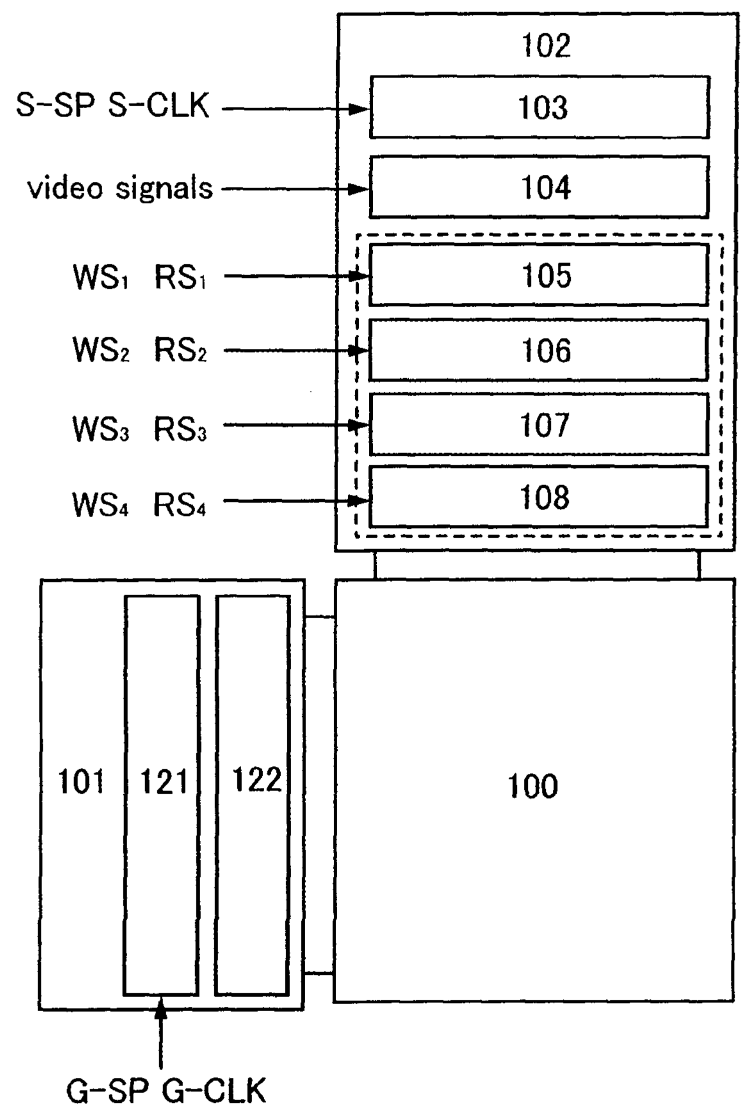
100
101
102
103
104
105
106
107
108
S-SP S-CLK
video signals
WS1 RS1
WS2 RS2
WS3 RS3
WS4 RS4
G-SP G-CLK
A-CLK
110
111
112
113
114
Hsync
Vsync
CLK
video data

FIG. 10



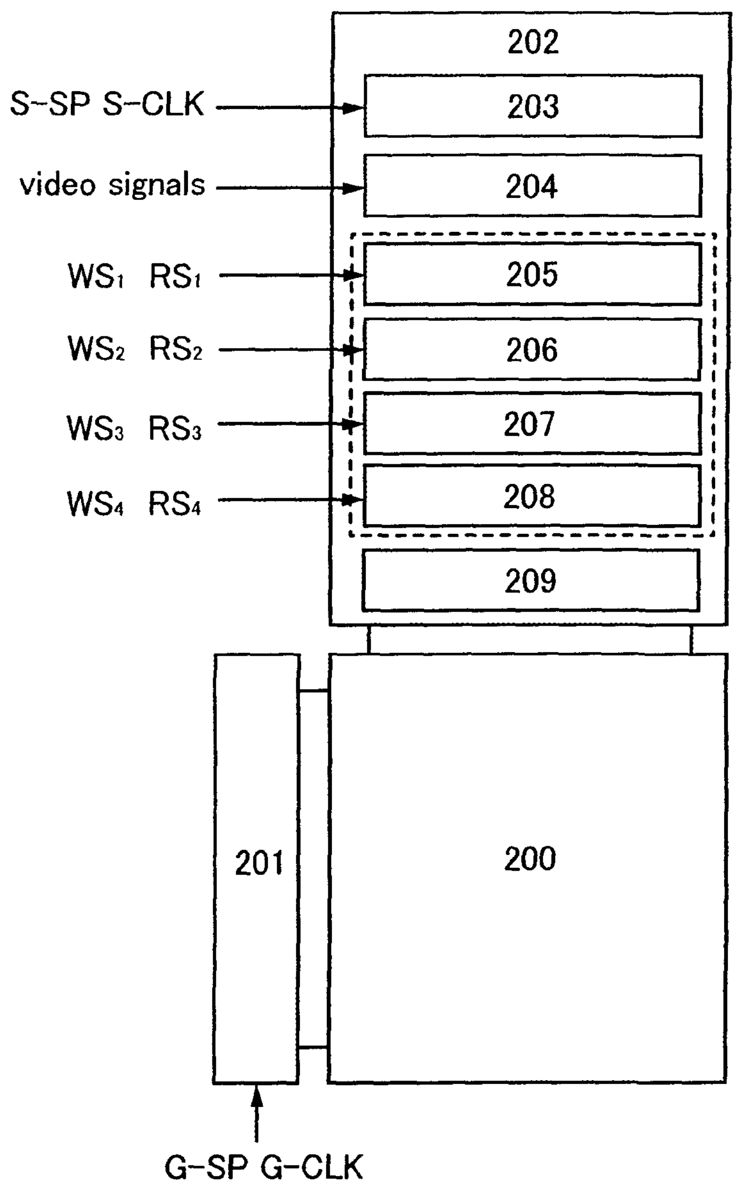
A-CLK
110
115
116
117
118
119
120
video signals of j-th line period
latch signal
102
timing control signal
113
video signals of j-th line period
video signals of (j+p)-th line period

FIG. 11



102
S-SP S-CLK
103
video signals
104
WS1 RS1
105
WS2 RS2
106
WS3 RS3
107
WS4 RS4
108
101
121
122
100
G-SP G-CLK

FIG. 12



202
S-SP S-CLK
203
video signals
204
WS1 RS1
205
WS2 RS2
206
WS3 RS3
207
WS4 RS4
208
209
201
200
G-SP G-CLK

FIG. 13A

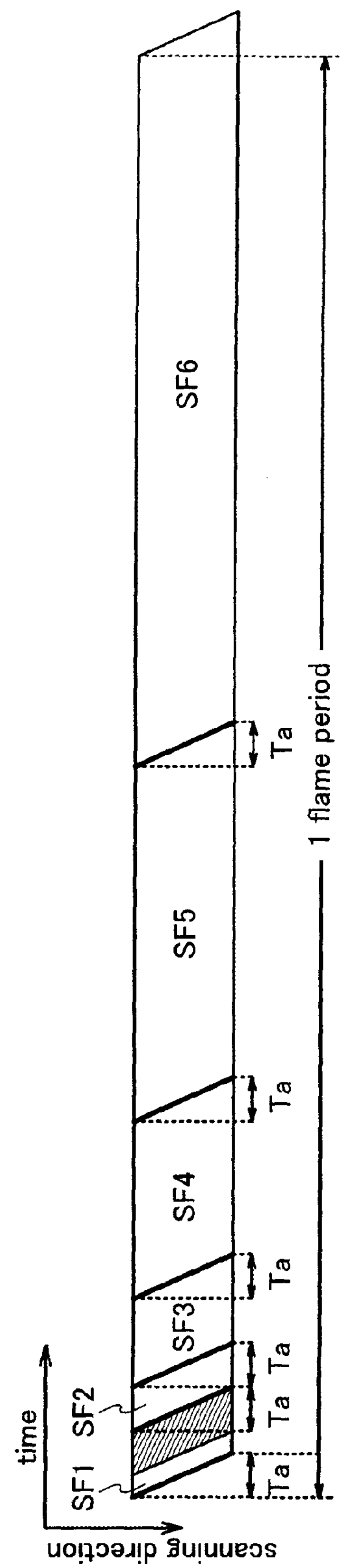


FIG. 13B

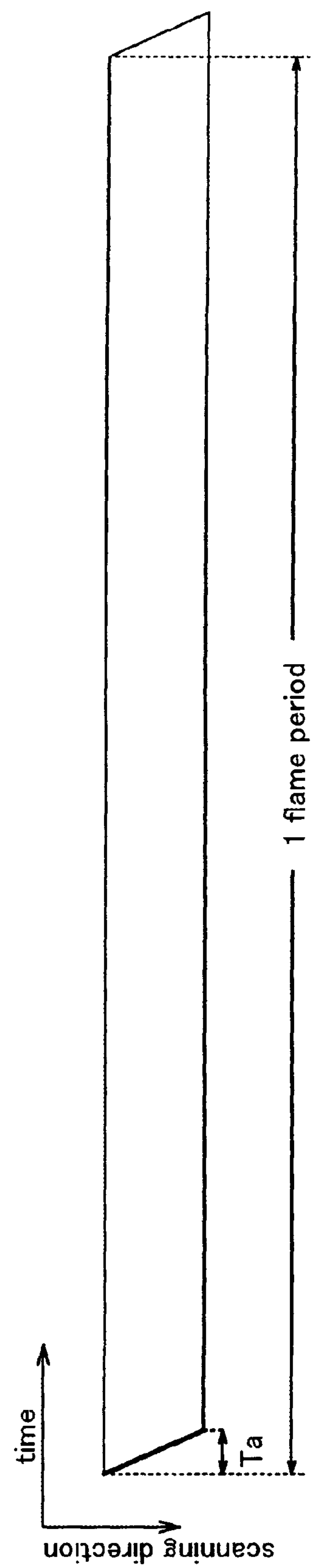


FIG. 14

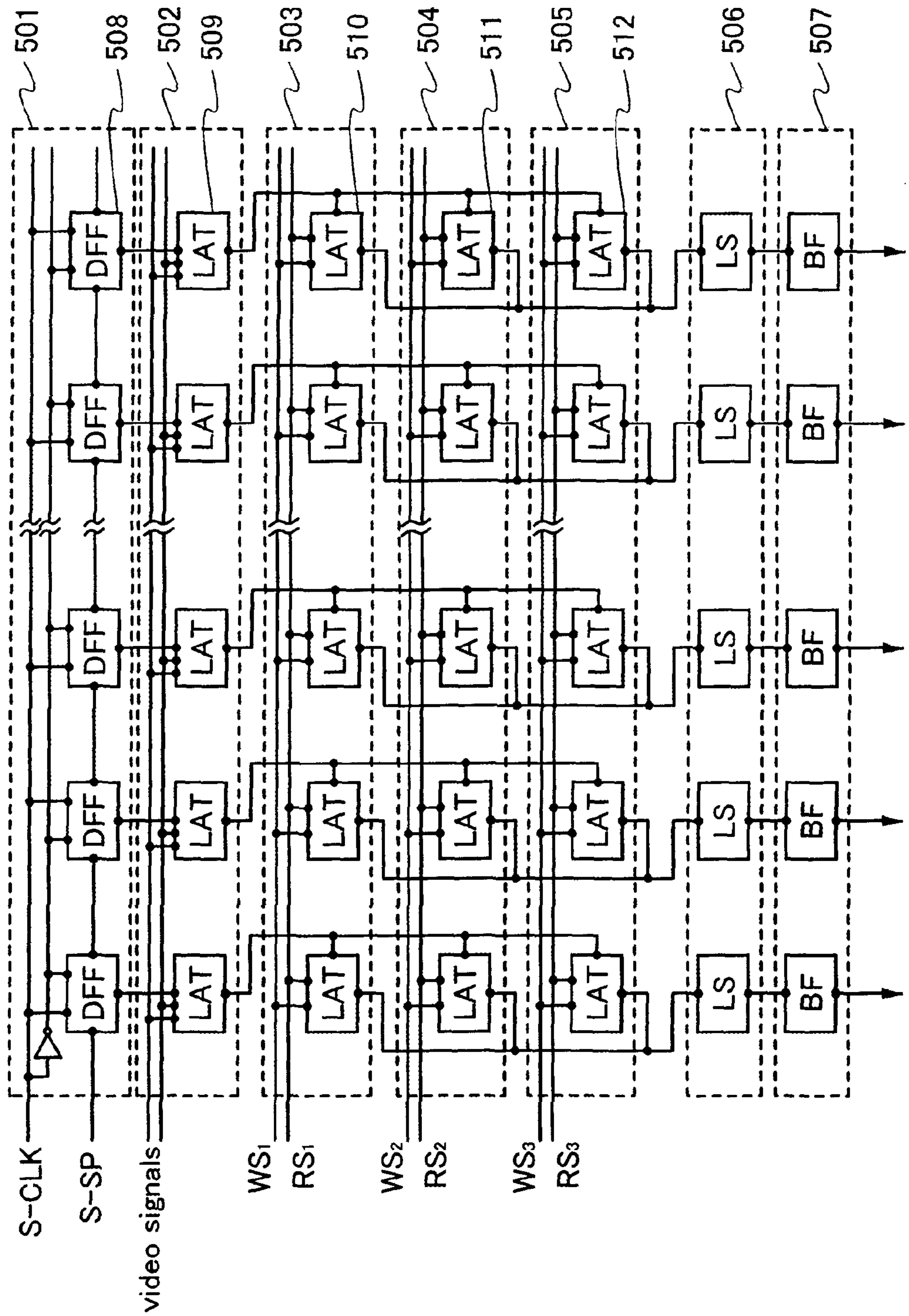

501
508
502
509
503
510
504
511
505
512
506
507
DFF
LAT
LS
BF
S-CLK
S-SP
video signals
WS1
RS1
WS2
RS2
WS3
RS3

FIG. 15

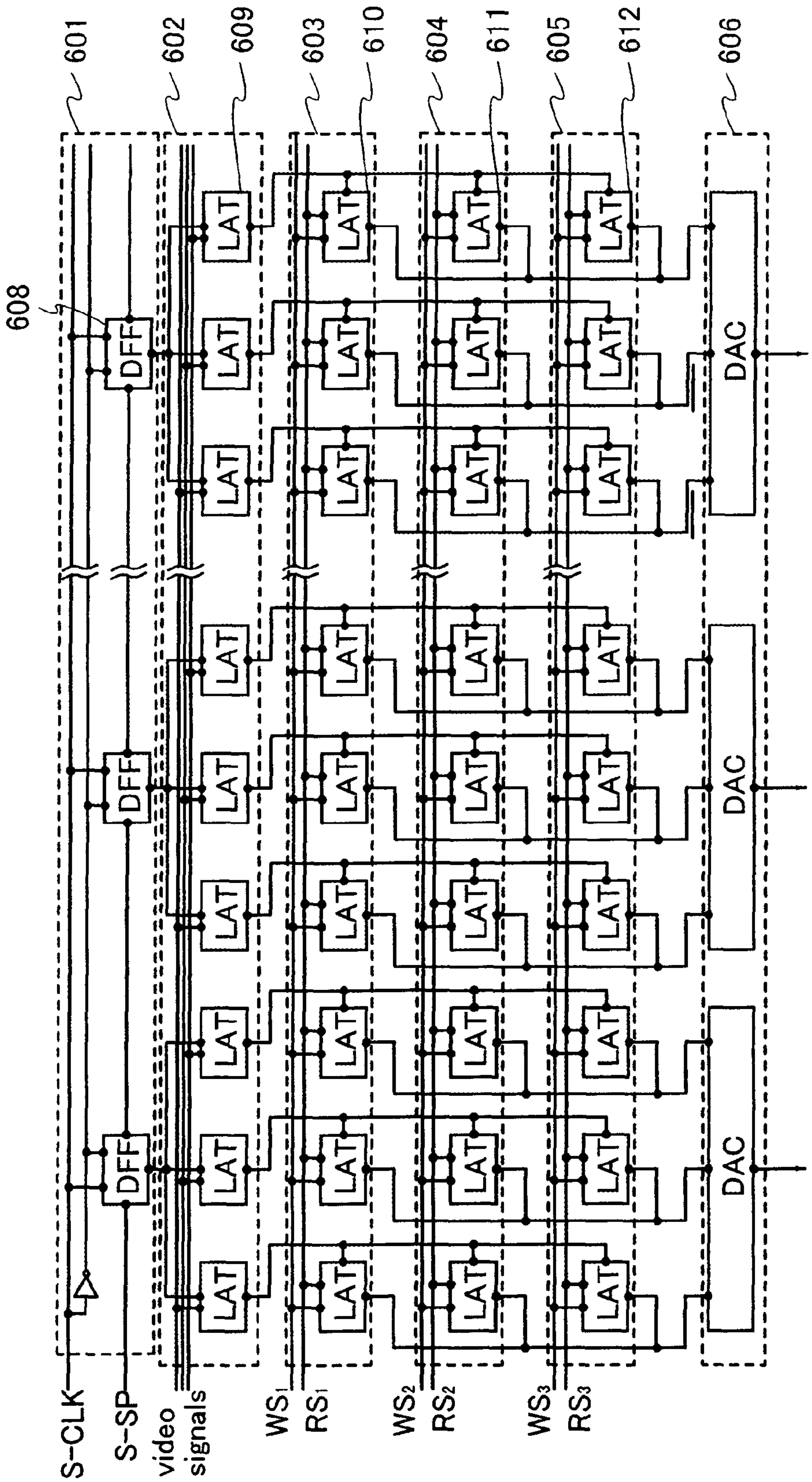

601
602
609
603
610
604
611
605
612
606
608
DFF
LAT
DAC
S-CLK
S-SP
video signals
WS_1
RS_1
WS_2
RS_2
WS_3
RS_3

FIG. 16A

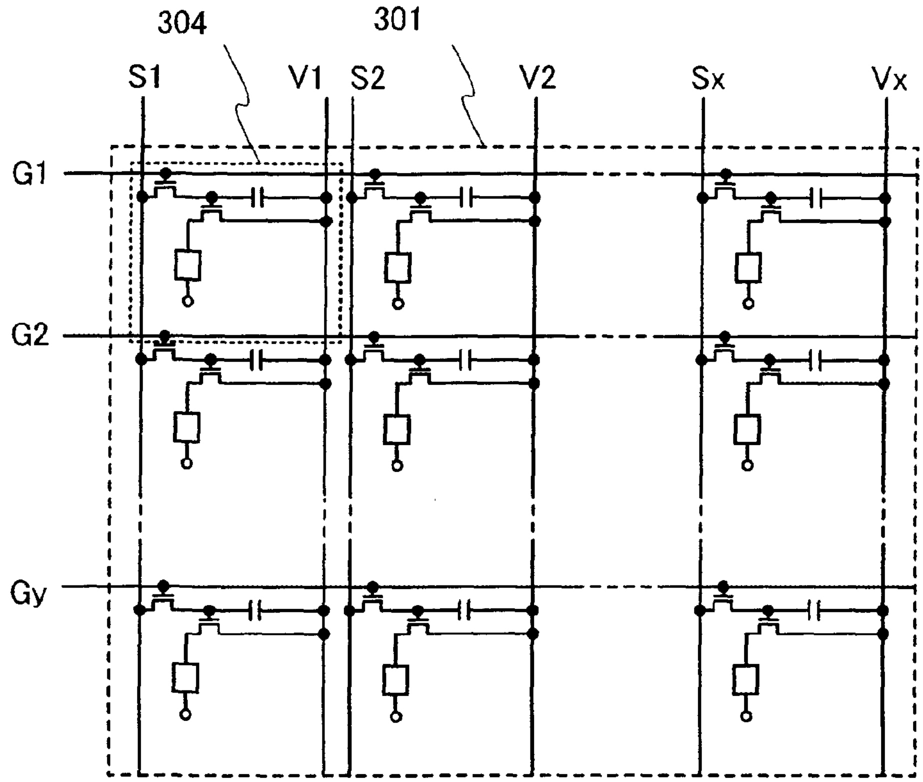


FIG. 16B

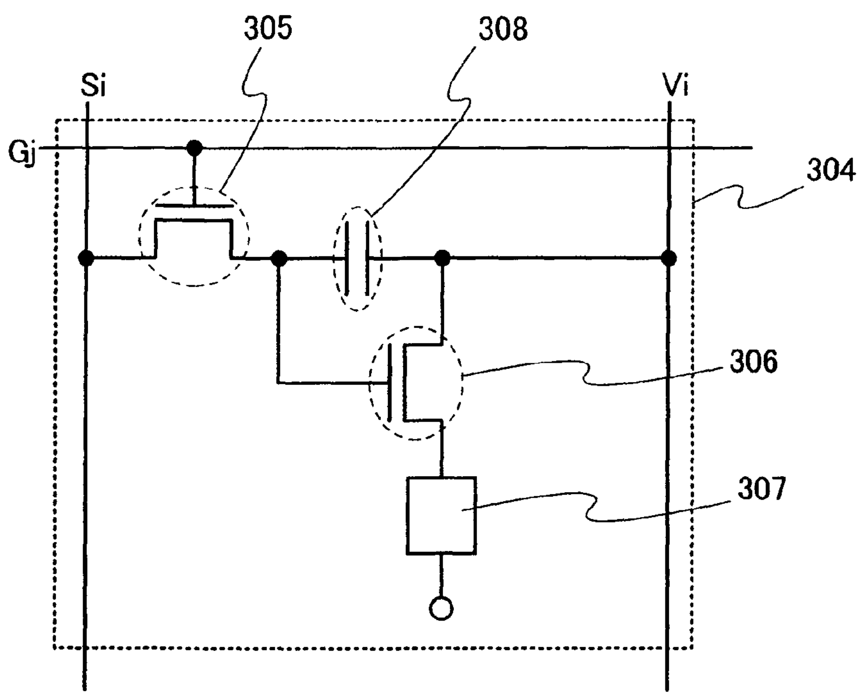


FIG. 17

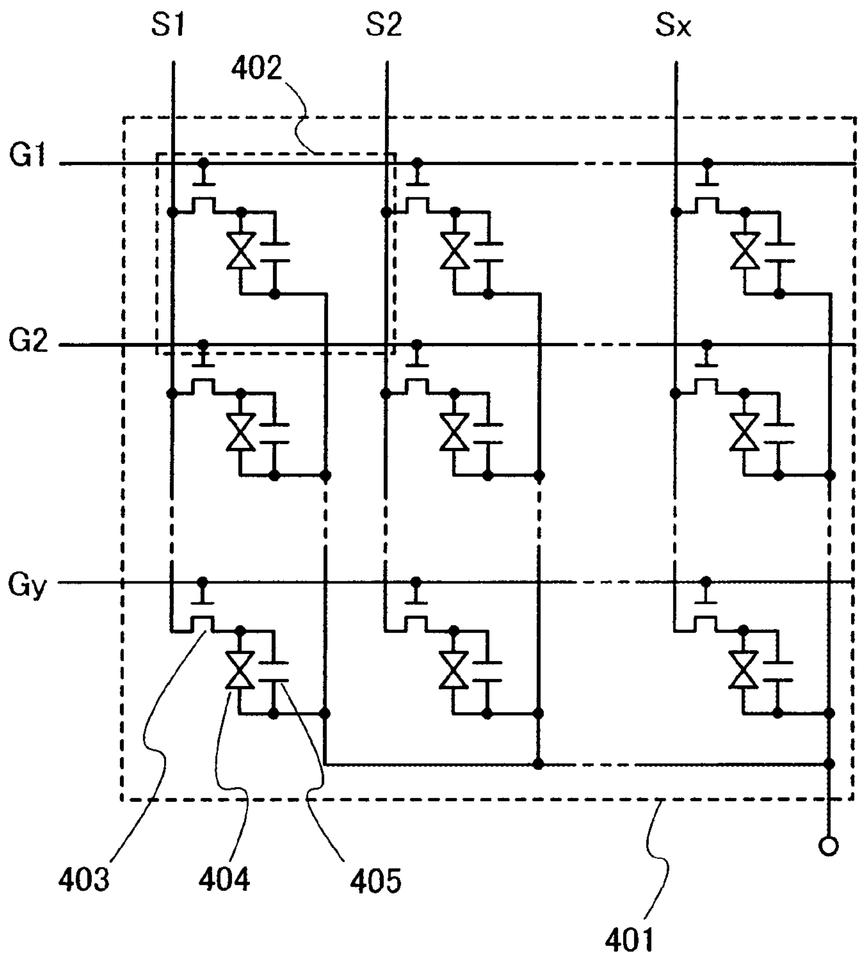


FIG. 18A

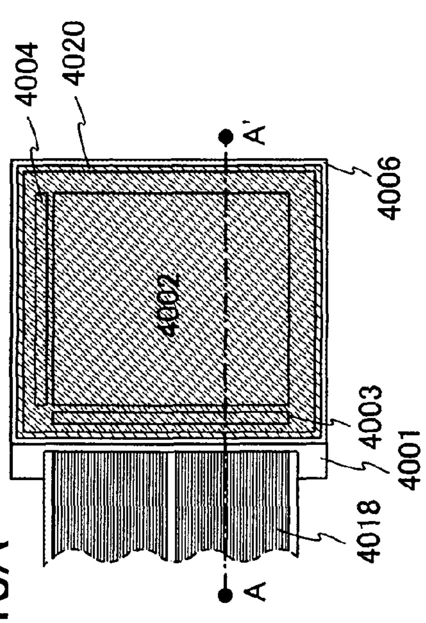


FIG. 18B

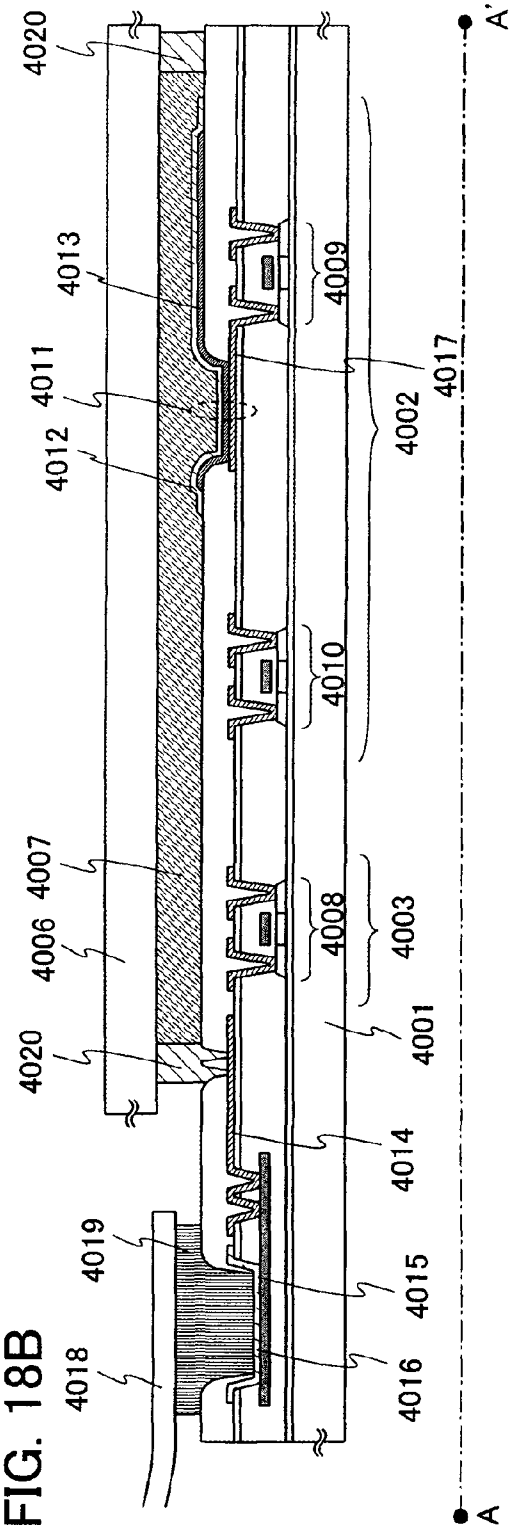


FIG. 19A

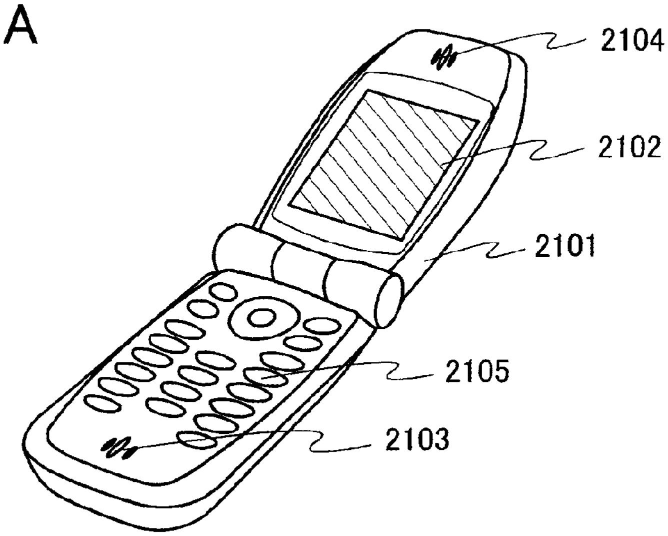


FIG. 19B

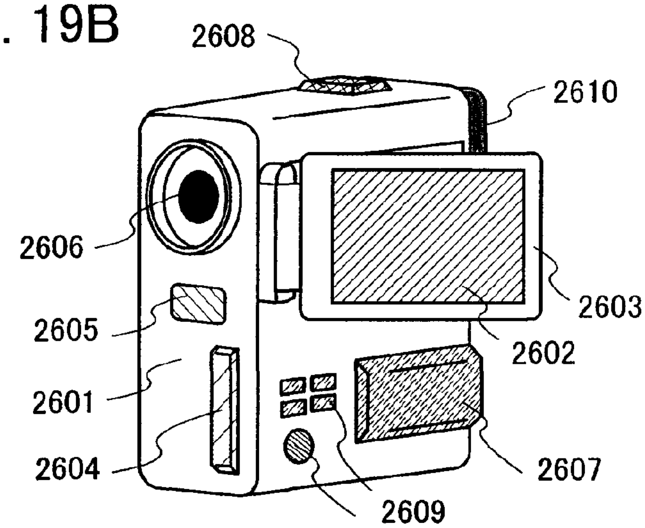


FIG. 19C

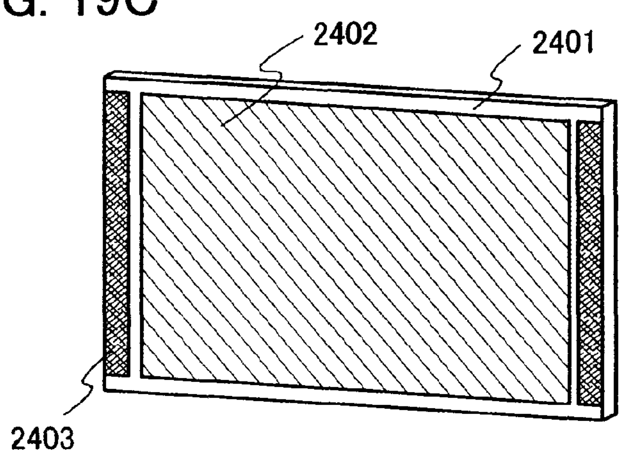


FIG. 20

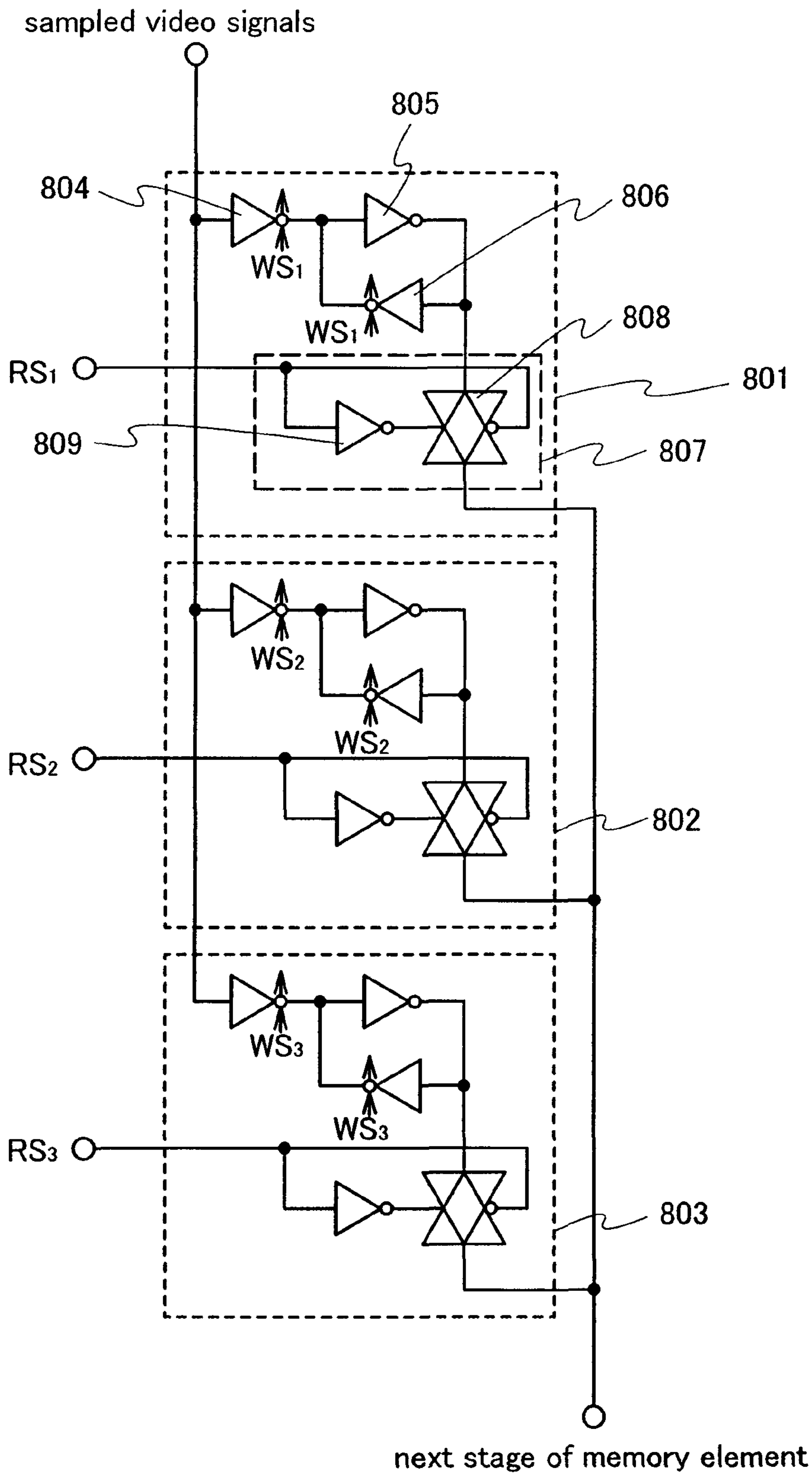

sampled video signals
805
804
806
WS1
WS1
808
RS1
801
809
807
WS2
WS2
RS2
802
WS3
WS3
RS3
803
next stage of memory element

FIG. 21

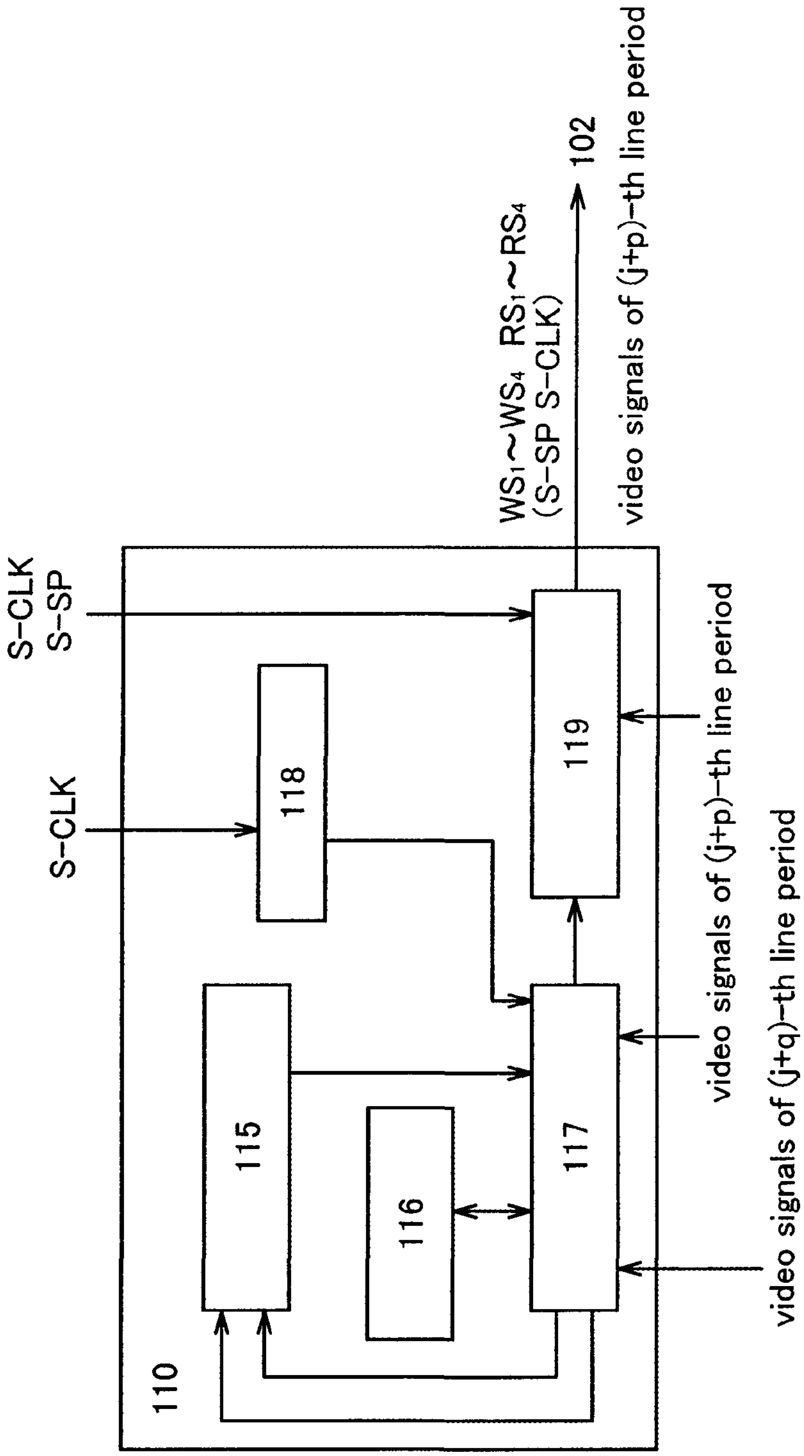
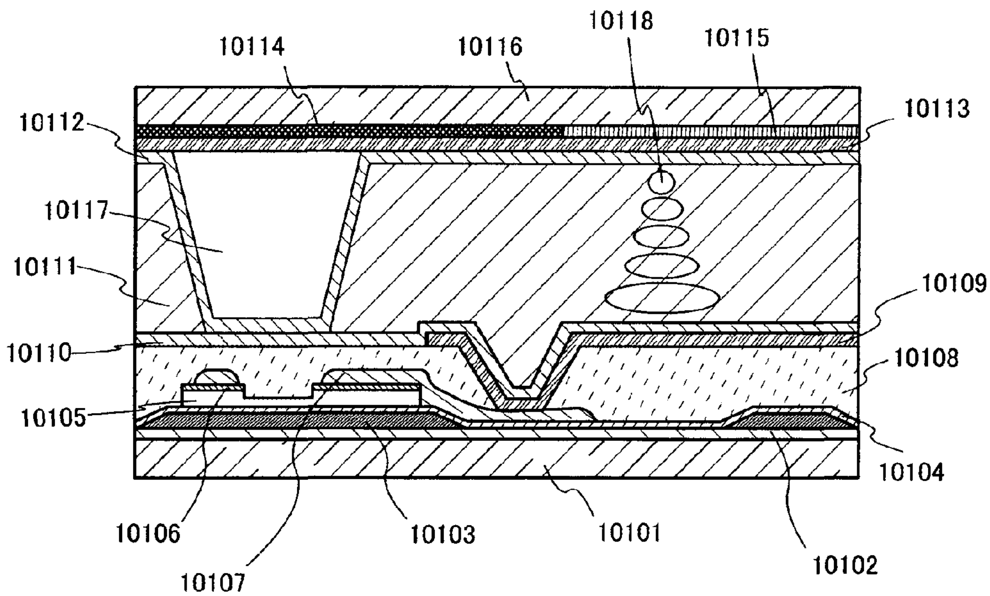

110
115
116
117
118
119
S-CLK
S-CLK
S-SP
$WS_1 \sim WS_4$ $RS_1 \sim RS_4$
(S-SP S-CLK)
102
video signals of (j+p)-th line period
video signals of (j+p)-th line period
video signals of (j+p)-th line period
video signals of (j+q)-th line period

FIG. 22



10114
10116
10118
10115
10112
10113
10117
10111
10109
10110
10108
10105
10104
10106
10103
10101
10102
10107

FIG. 23A

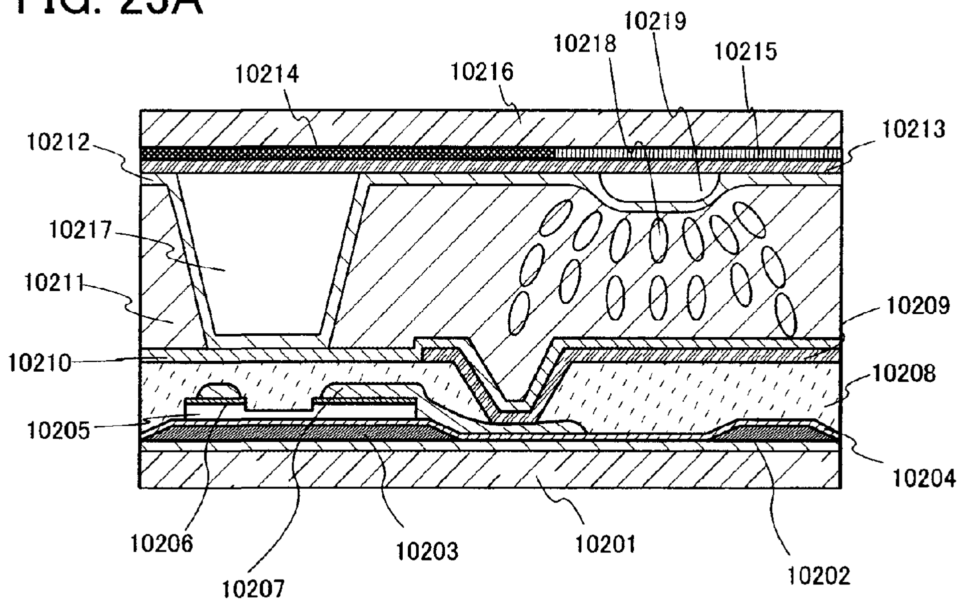


FIG. 23B

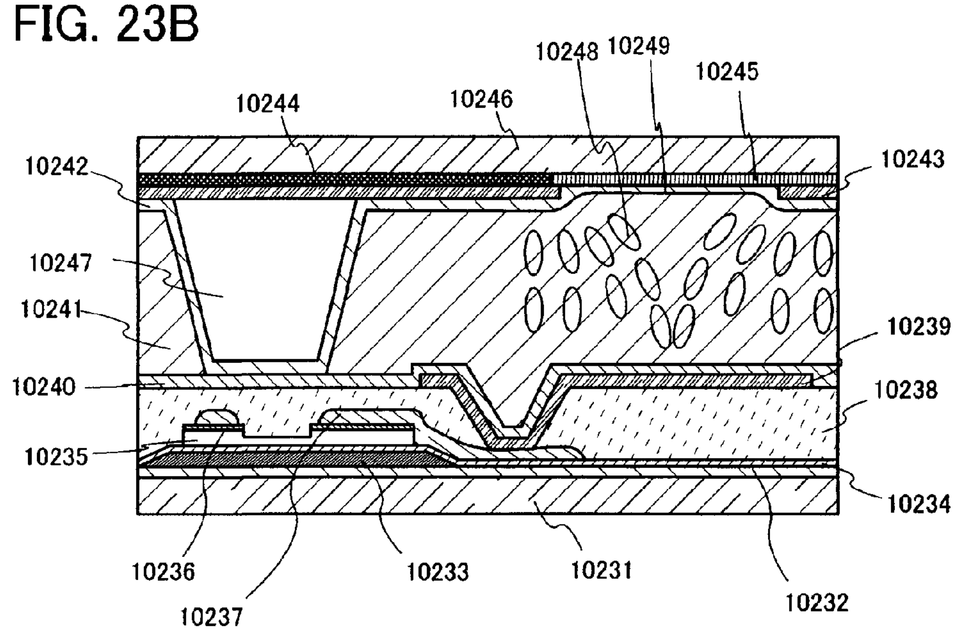


FIG. 24A

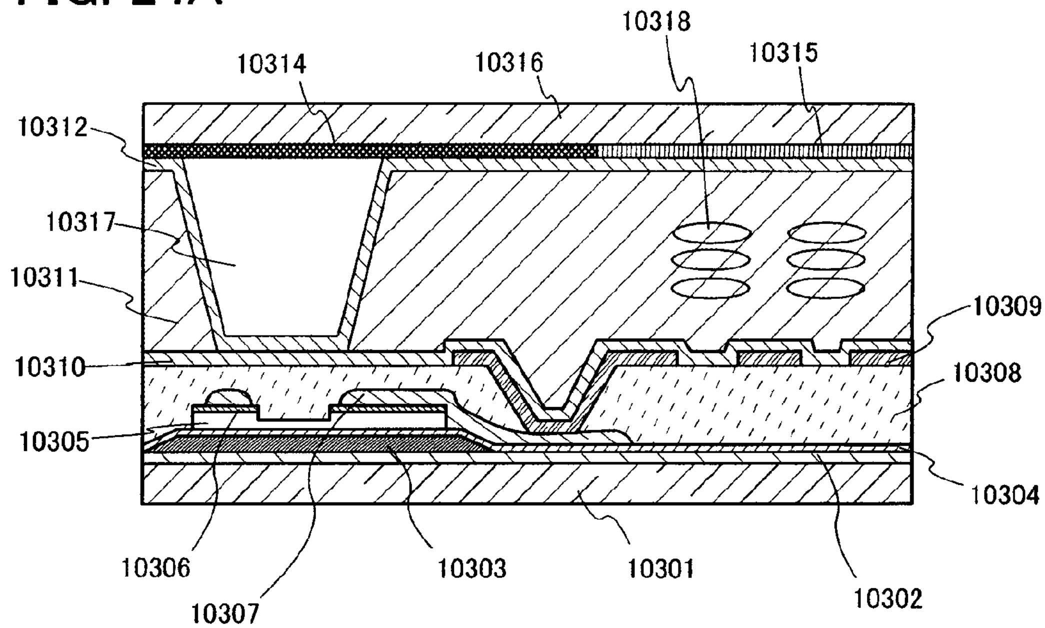


FIG. 24B

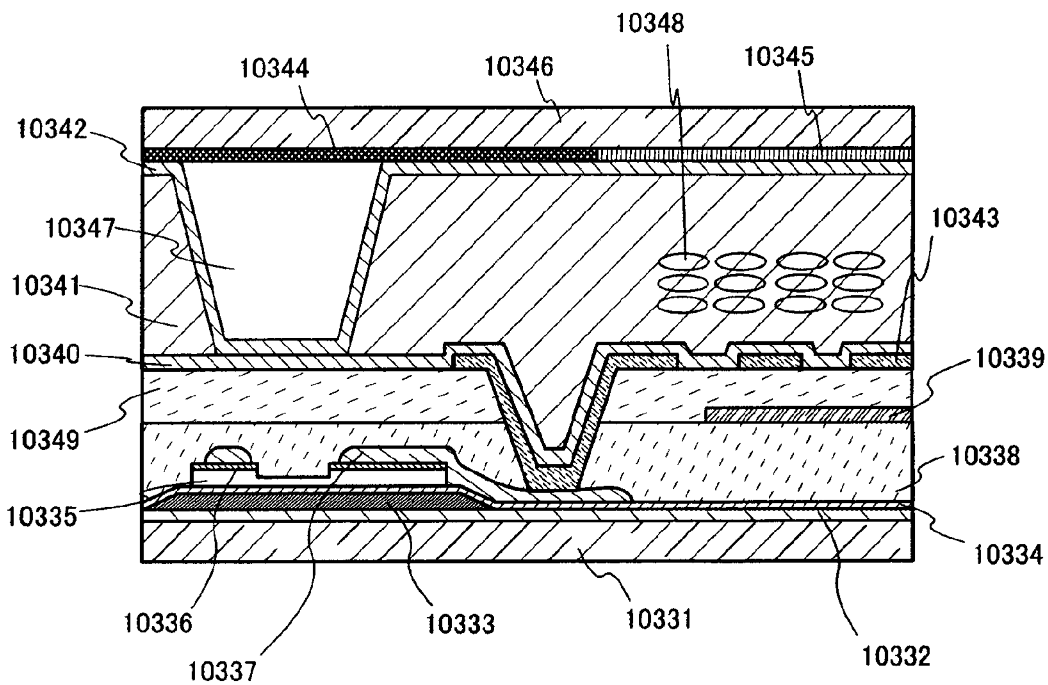
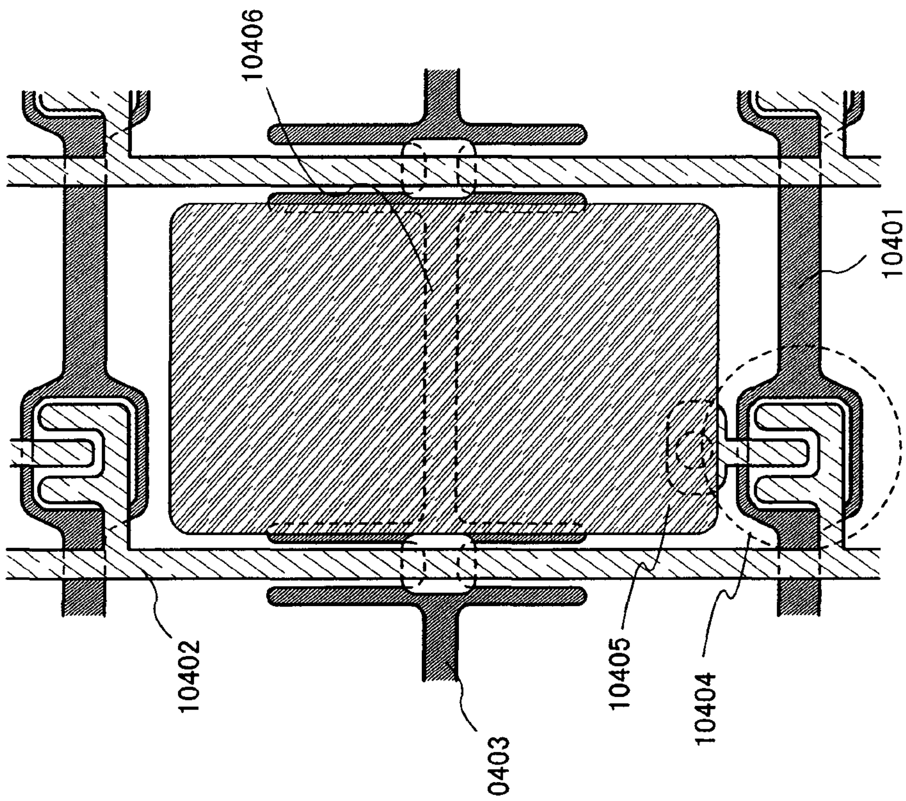


FIG. 25



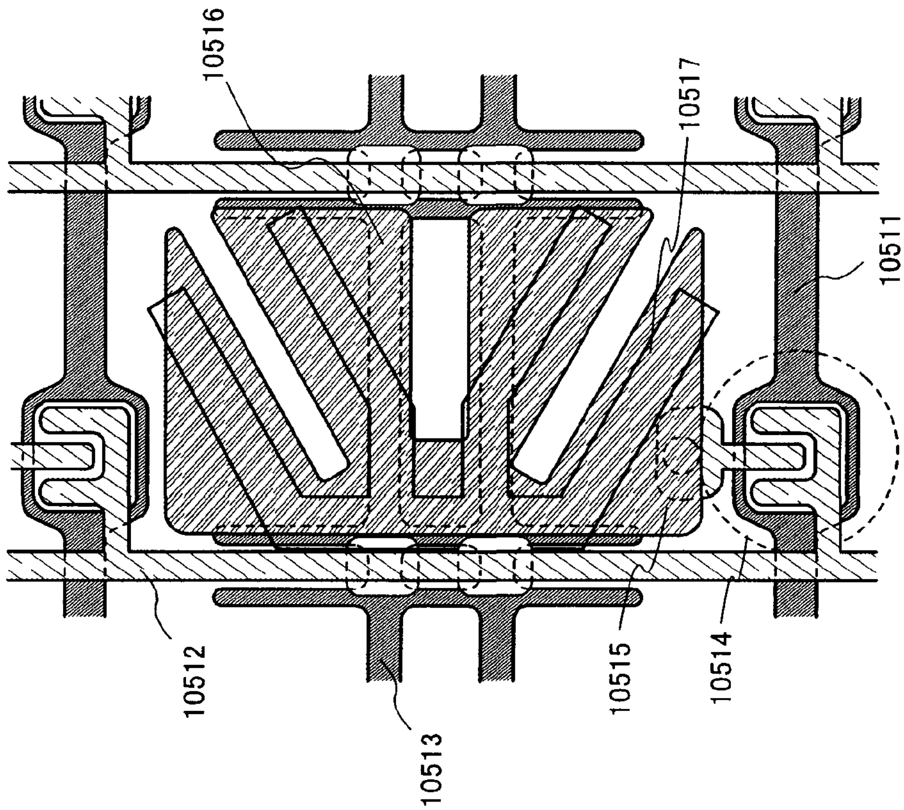


FIG. 26B

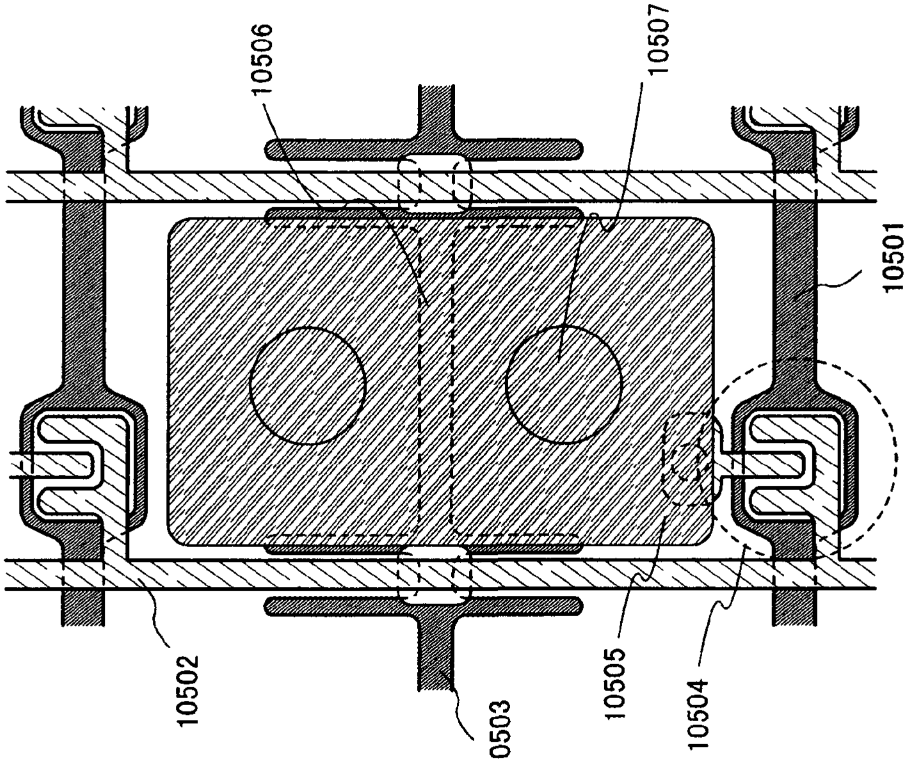


FIG. 26A

FIG. 27B

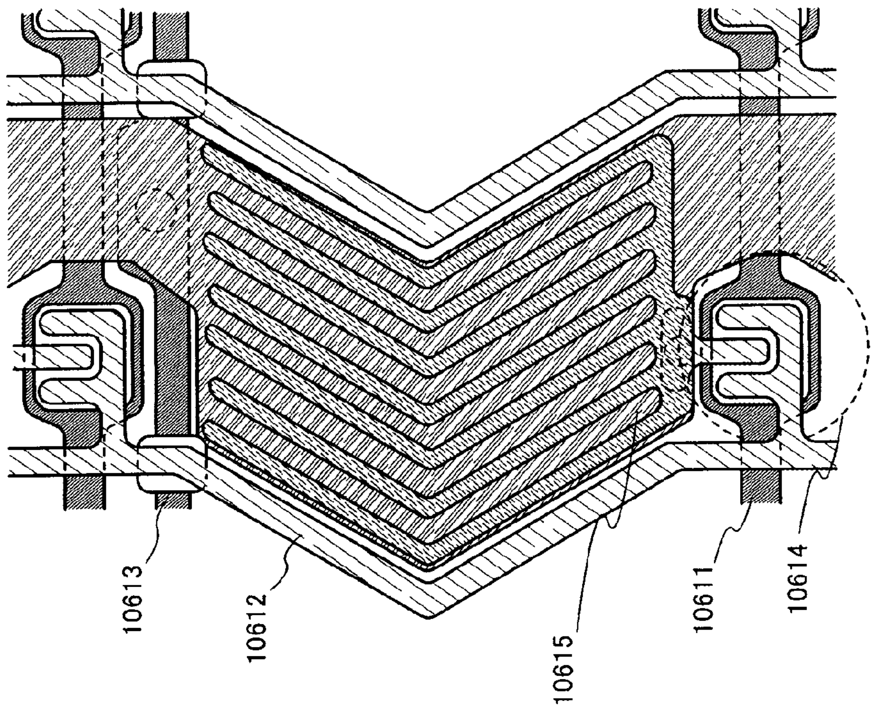
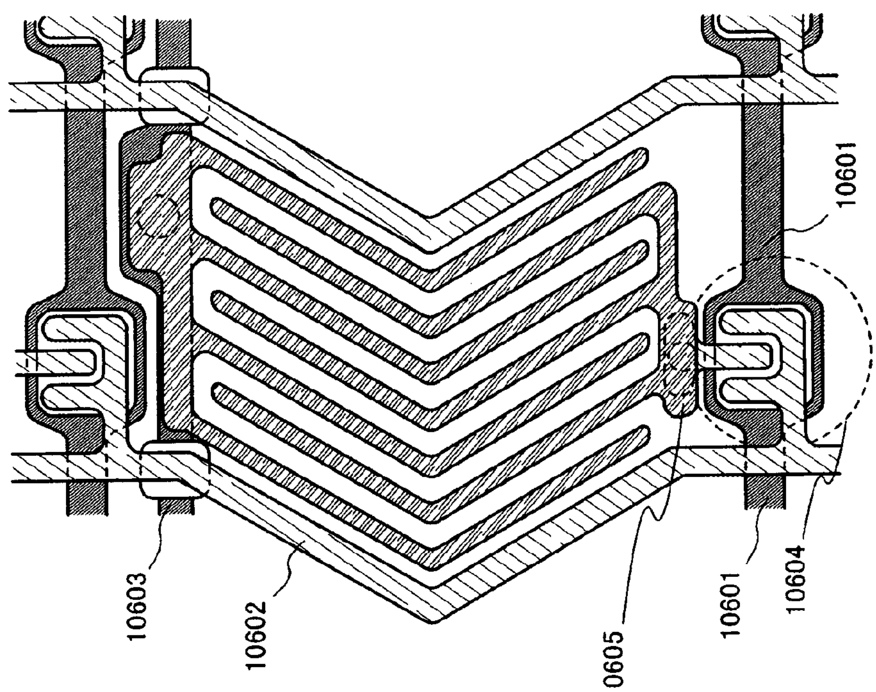


FIG. 27A



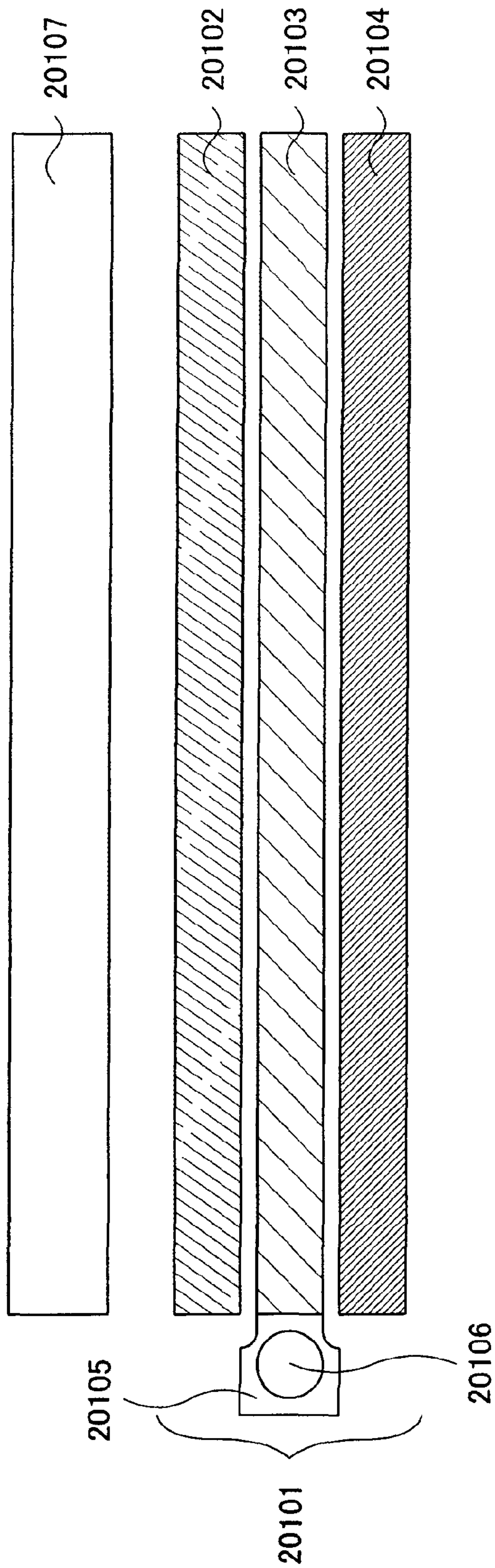


FIG. 28

FIG. 29A

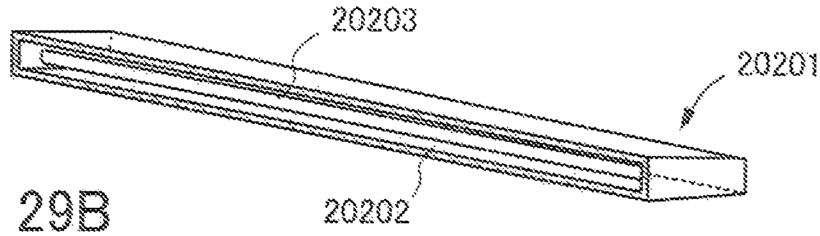


FIG. 29B

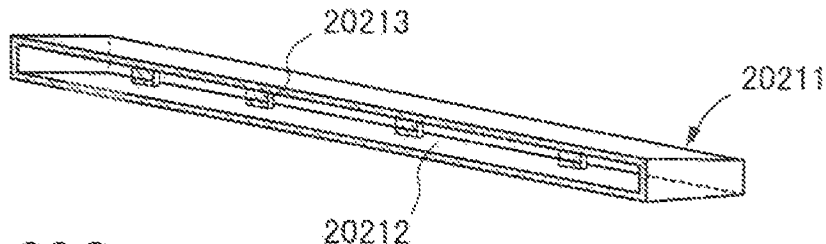


FIG. 29C

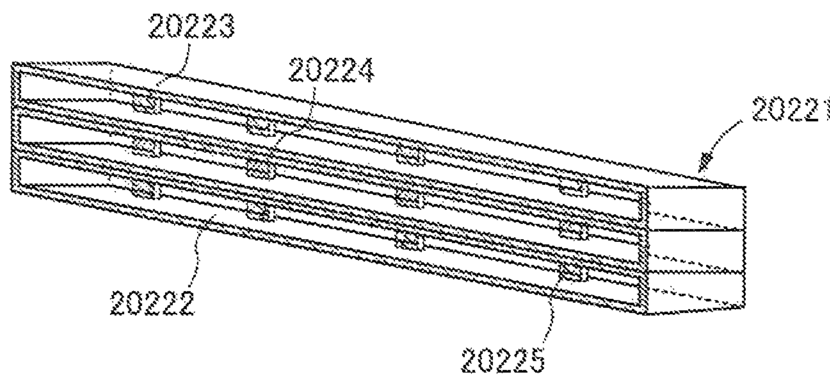


FIG. 29D

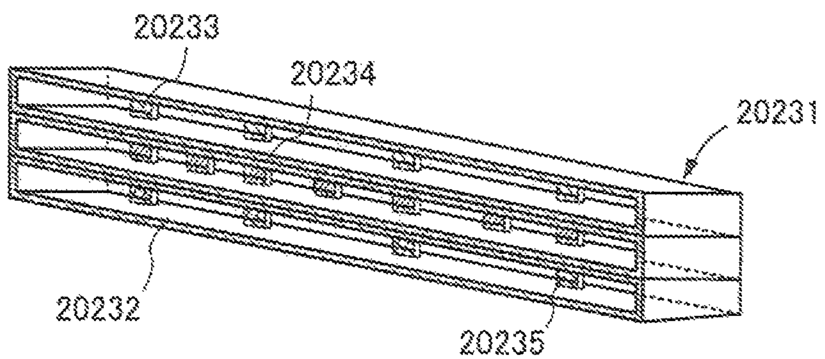


FIG. 30

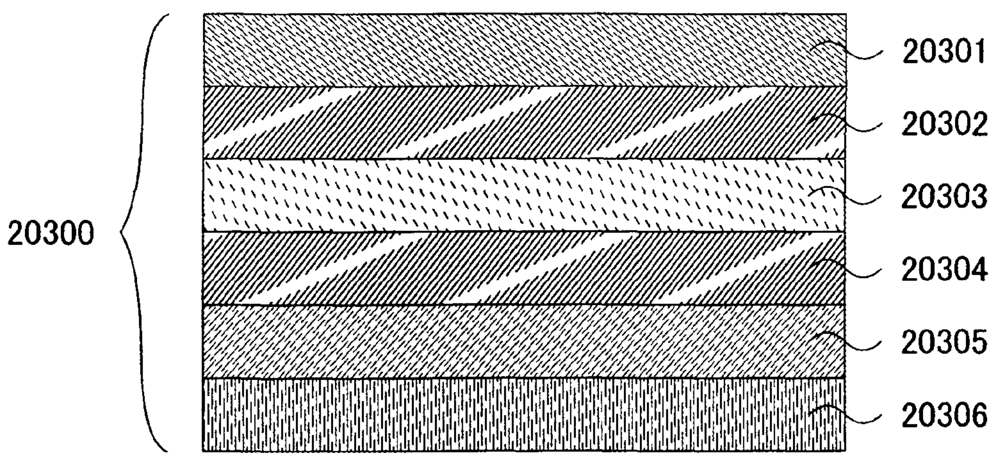


FIG. 31A

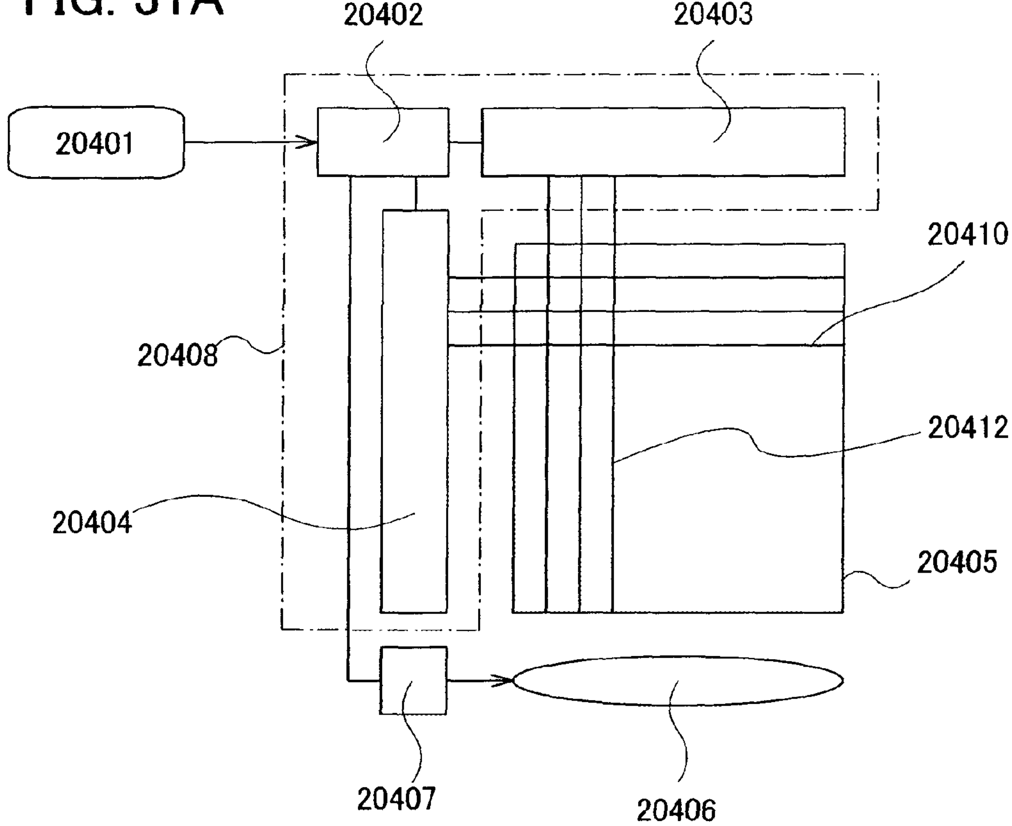


FIG. 31B

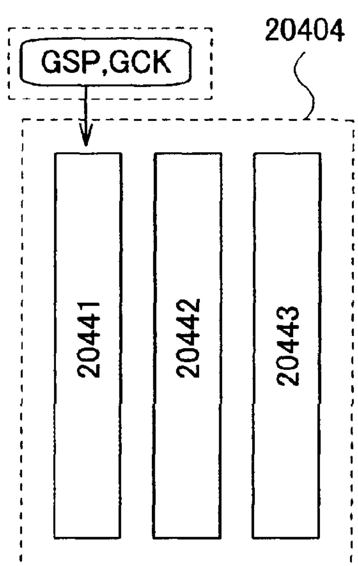
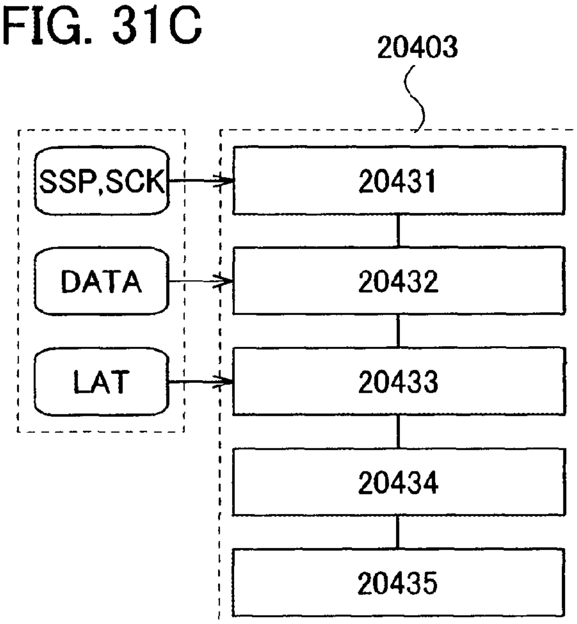


FIG. 31C



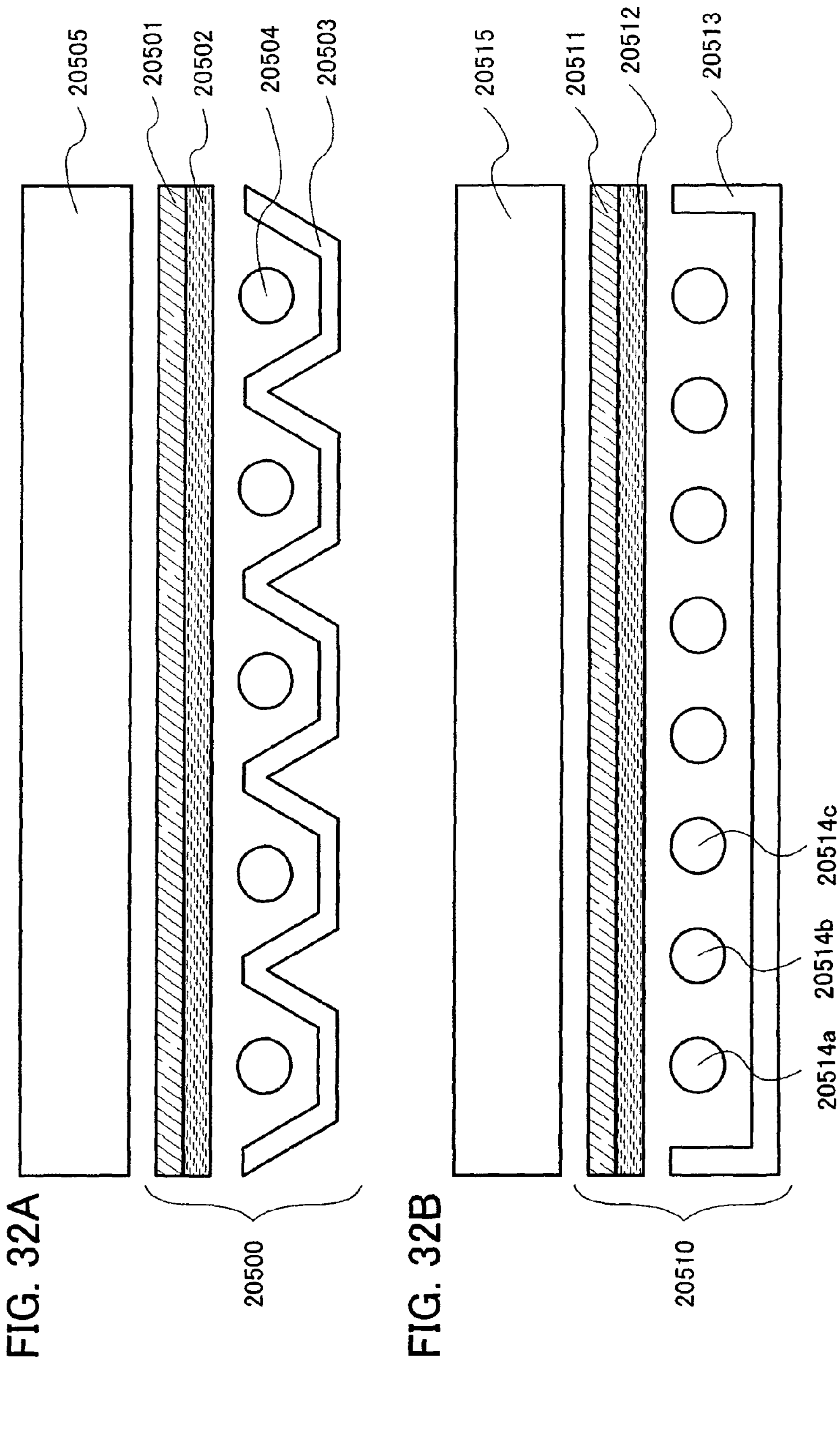


FIG. 32A

FIG. 32B

FIG. 33A

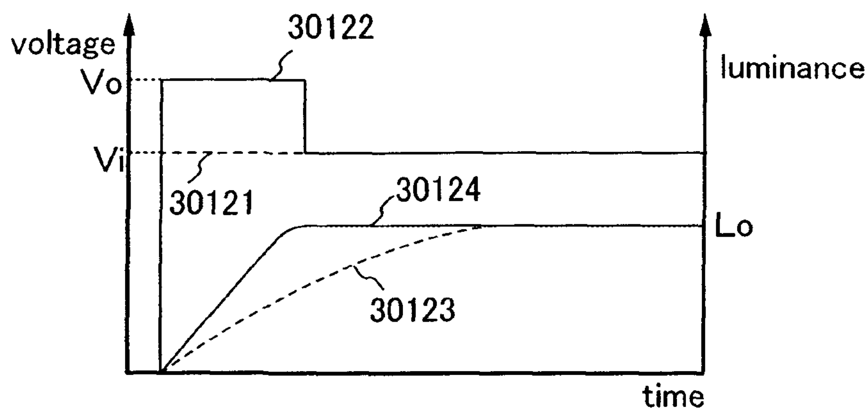


FIG. 33B

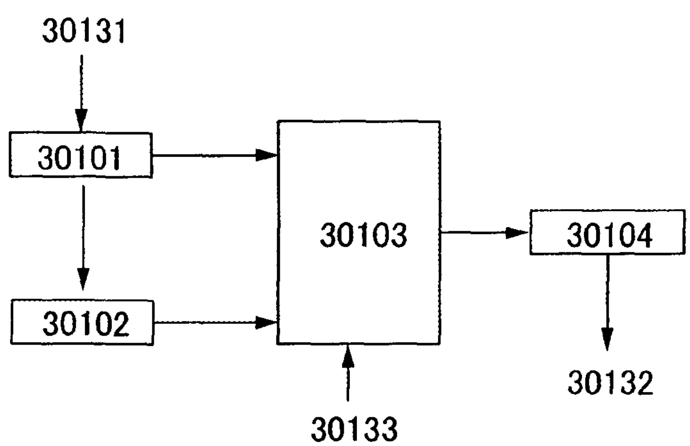


FIG. 33C

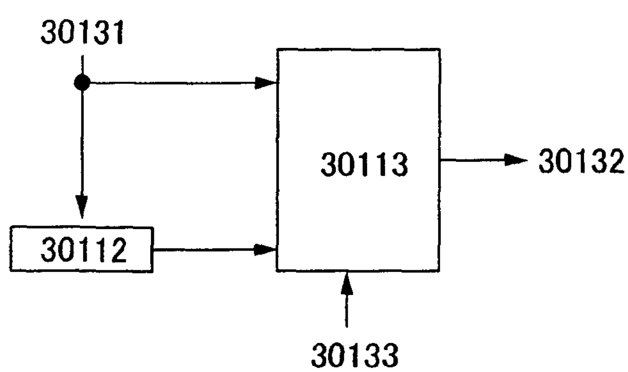


FIG. 34A

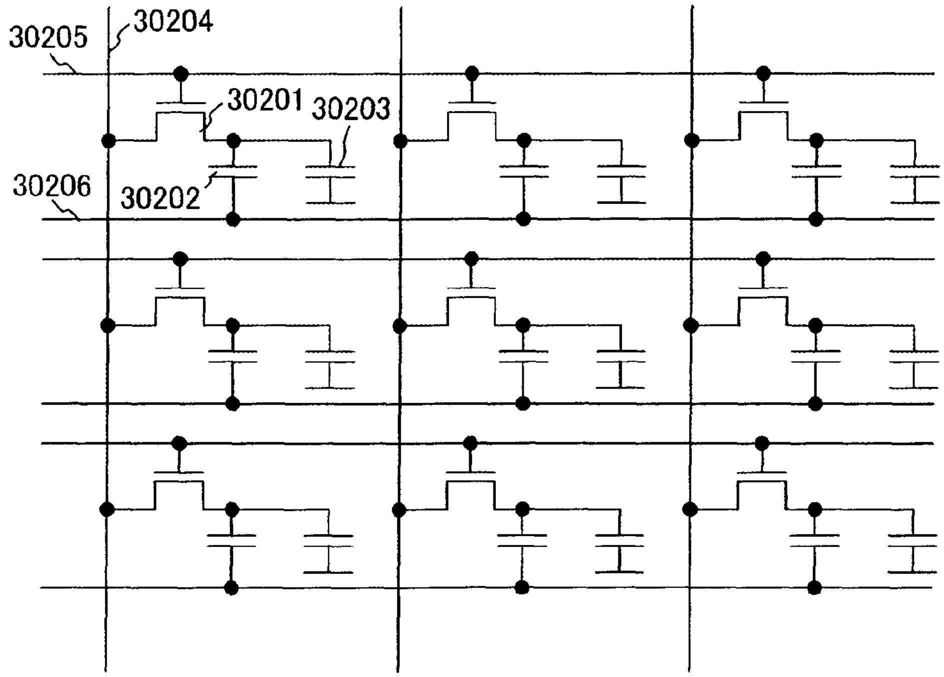


FIG. 34B

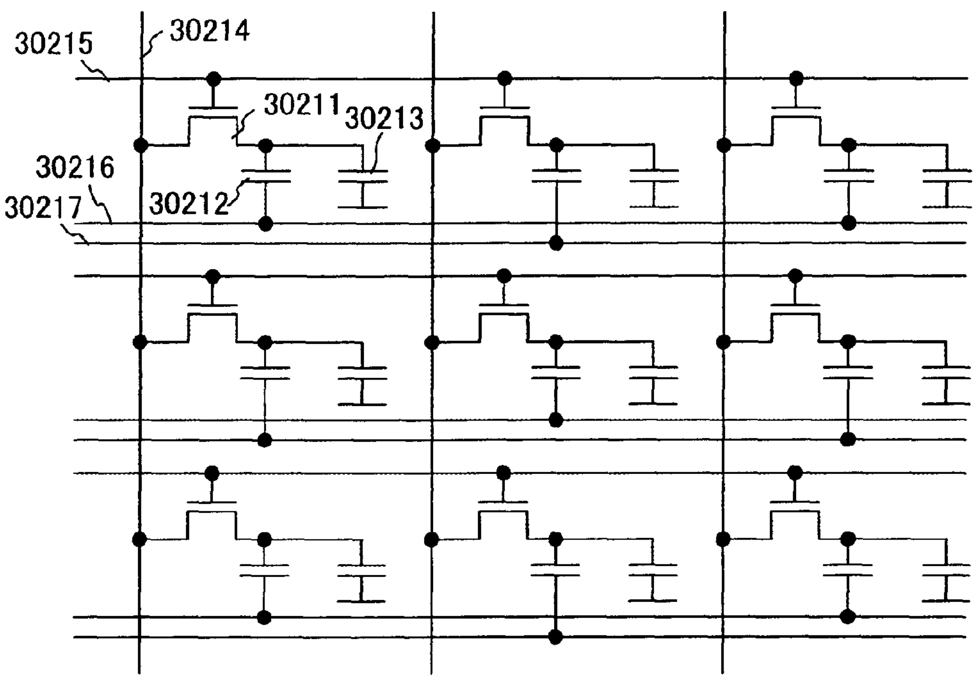


FIG. 35A

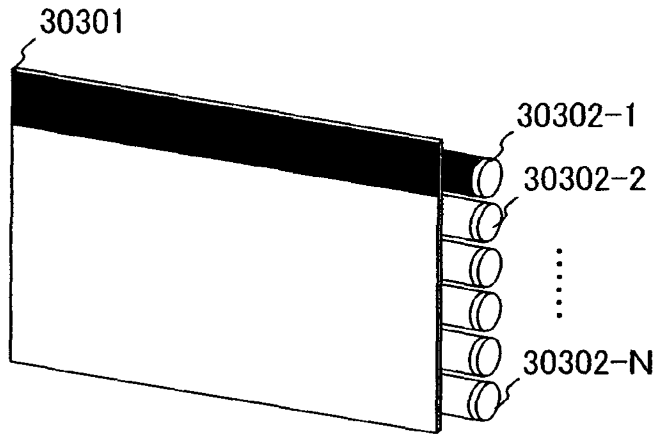


FIG. 35B

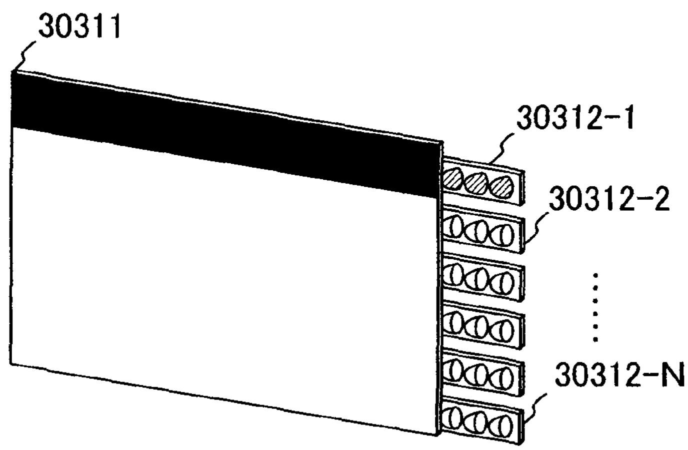


FIG. 35C

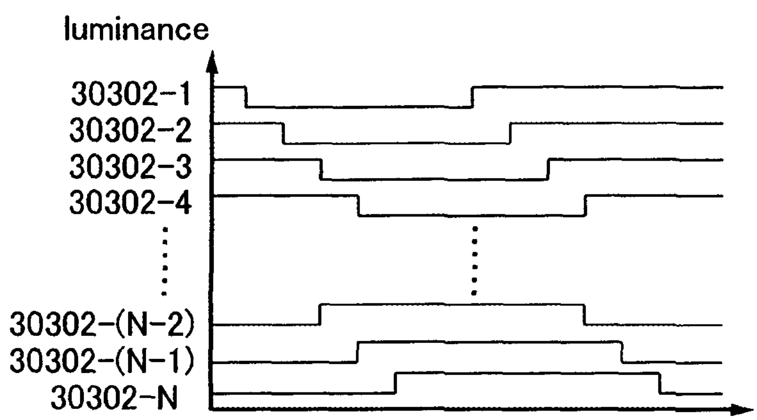


FIG. 36A

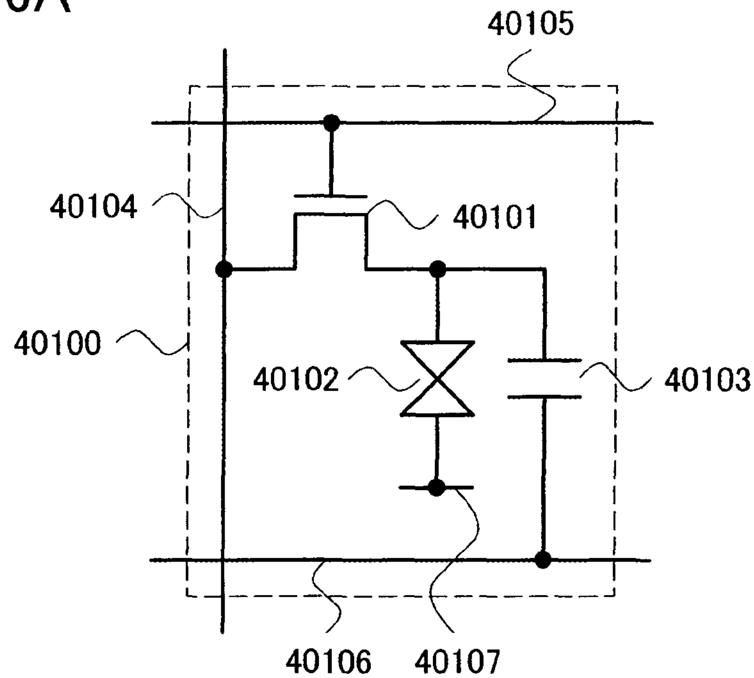


FIG. 36B

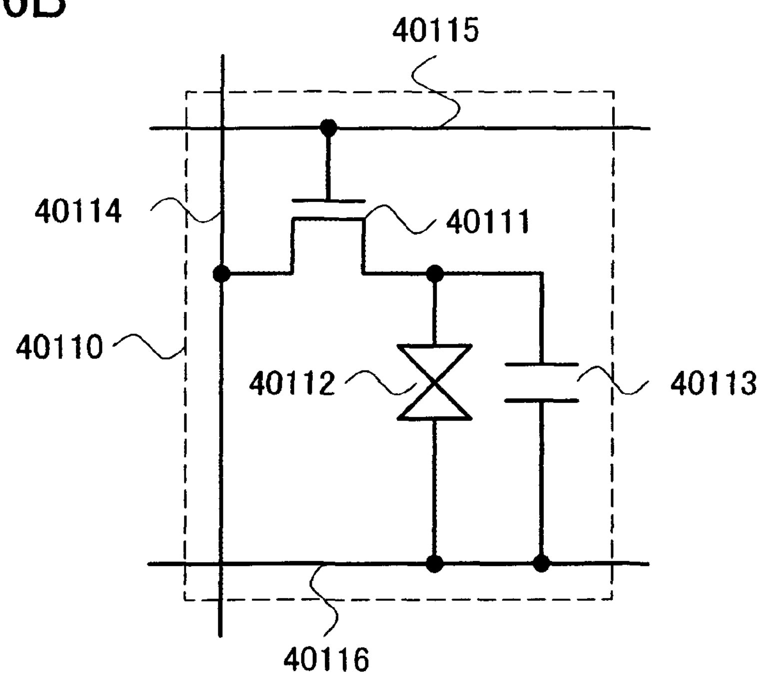


FIG. 37

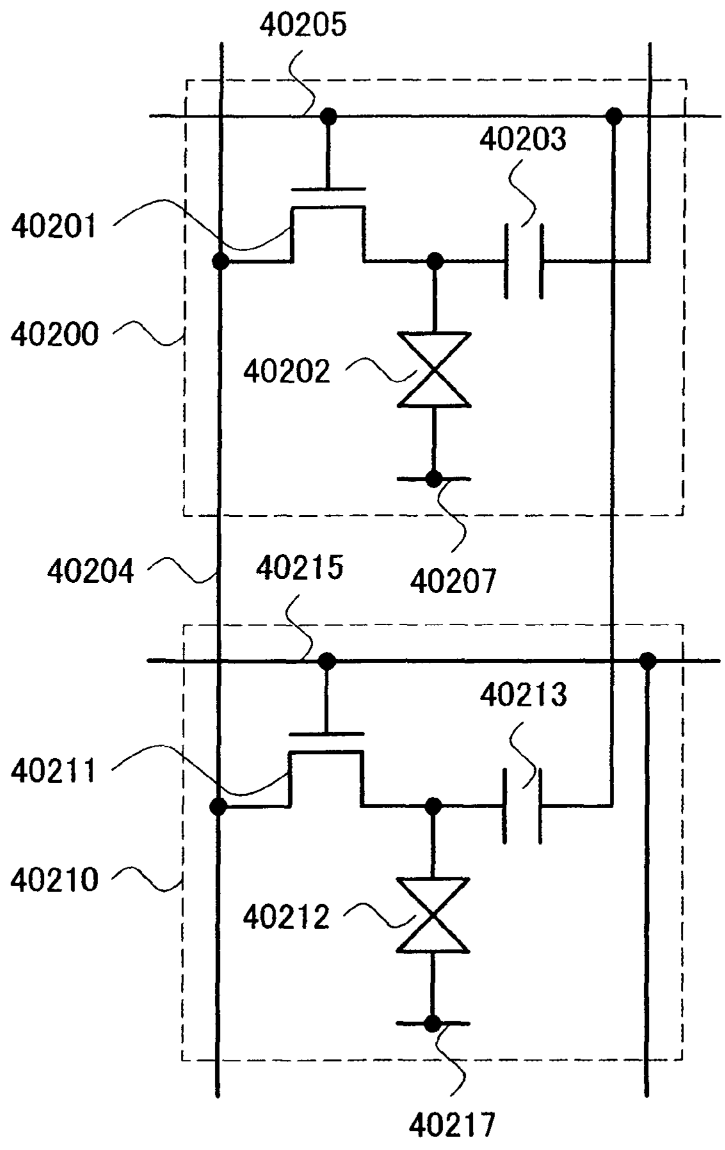

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FIG. 38

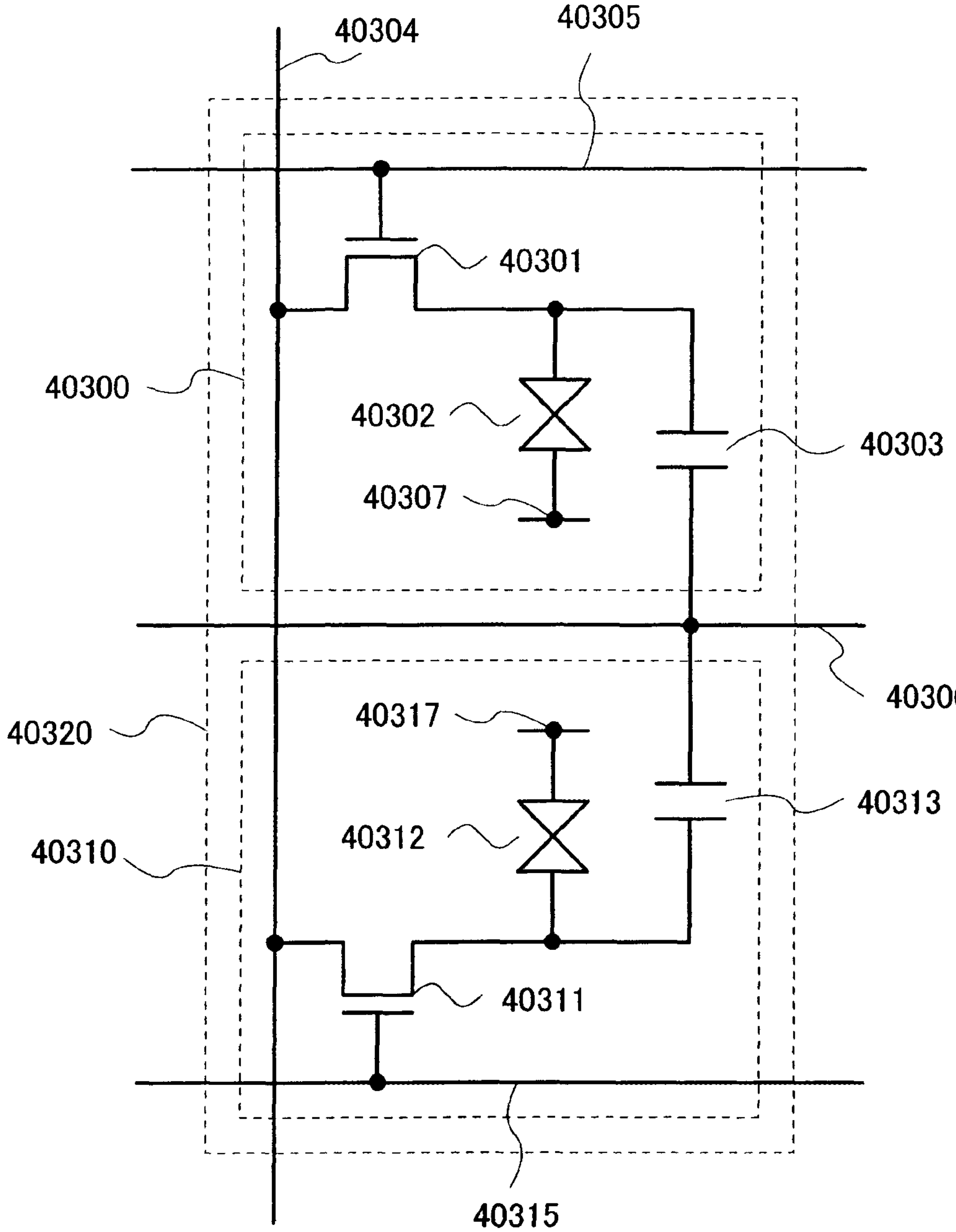
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FIG. 39A

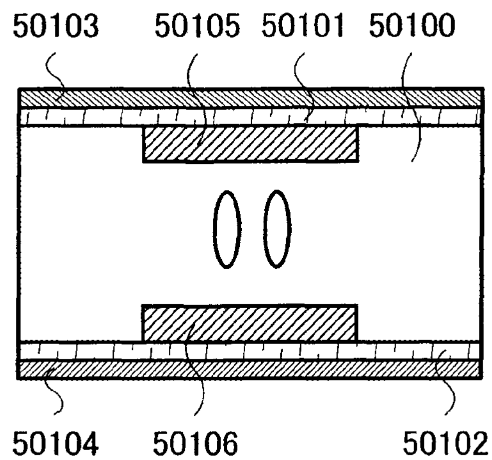

FIG. 39B

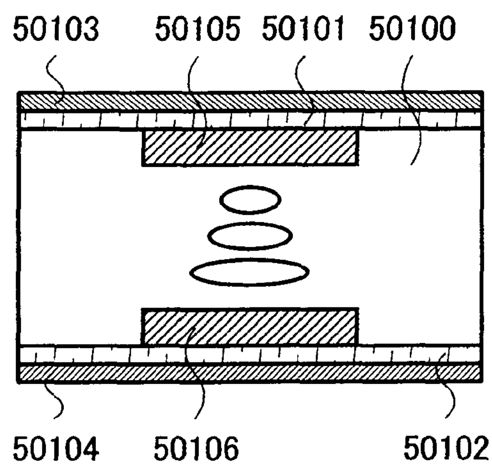

FIG. 40A

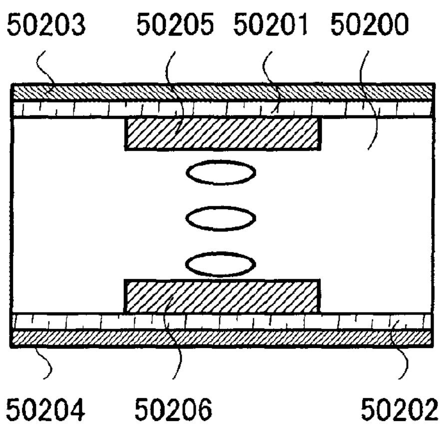

FIG. 40B

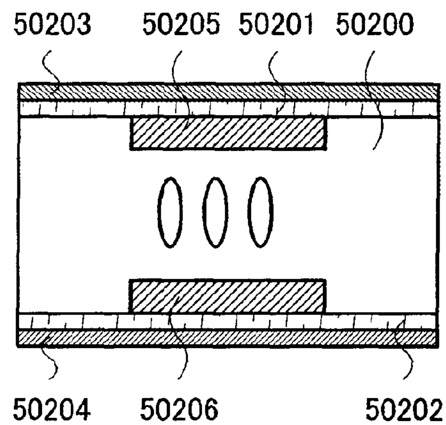

FIG. 40C

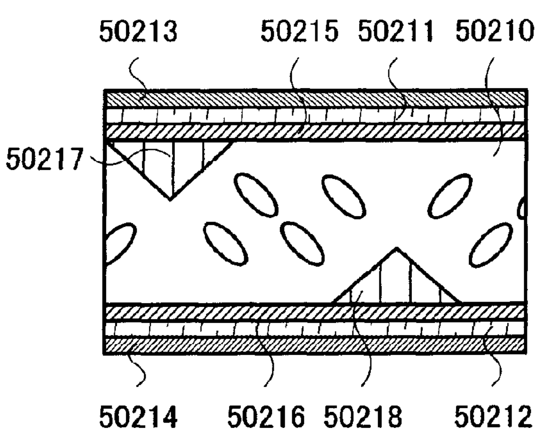

FIG. 40D

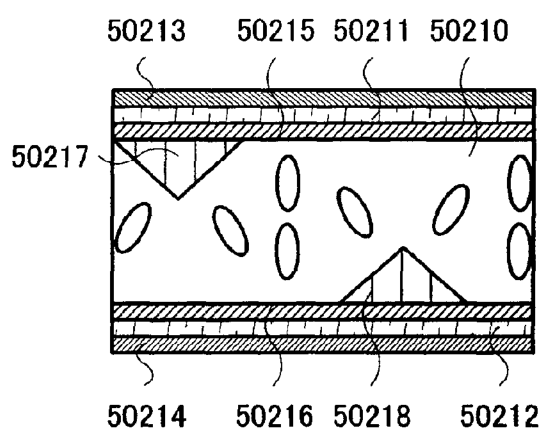

FIG. 41A

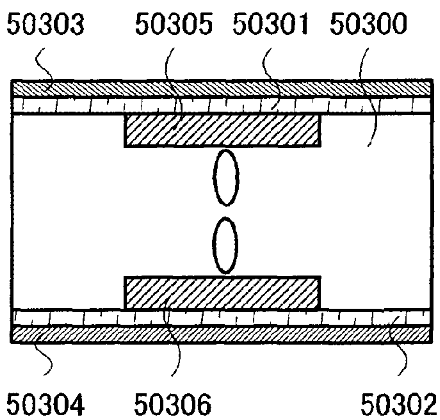

FIG. 41B

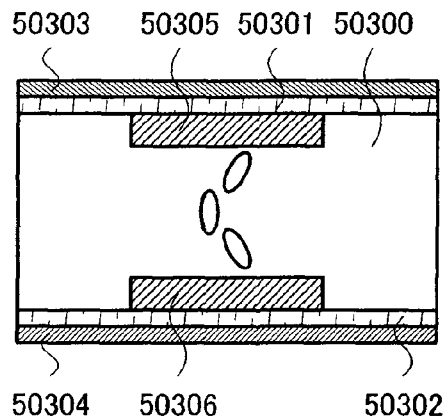

FIG. 41C

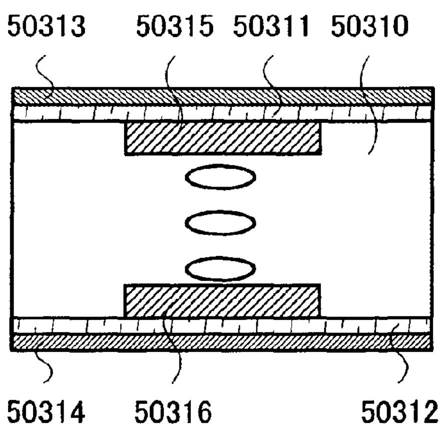

FIG. 41D

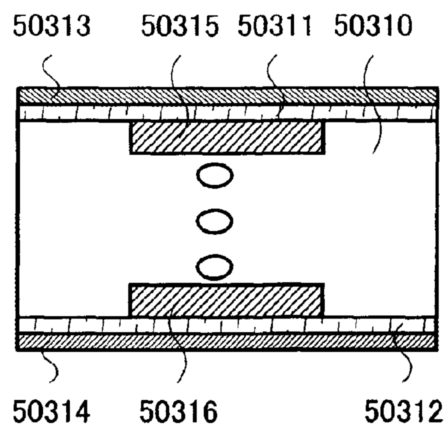

FIG. 42A

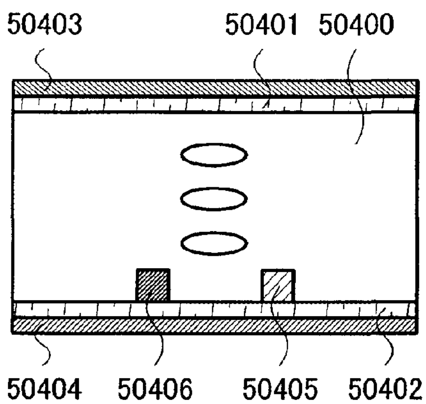

FIG. 42B

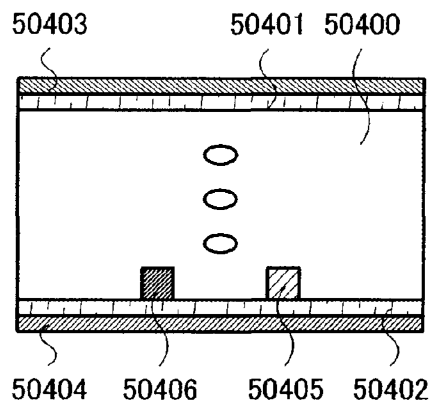

FIG. 42C

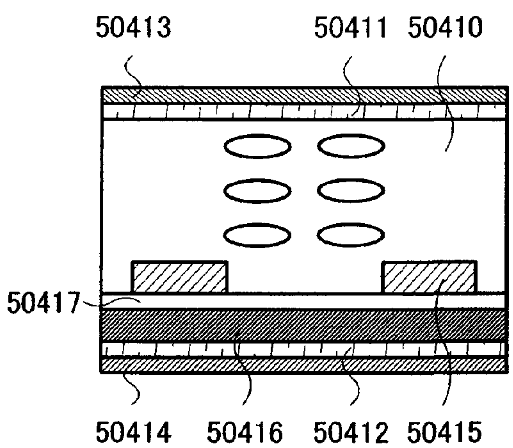

FIG. 42D

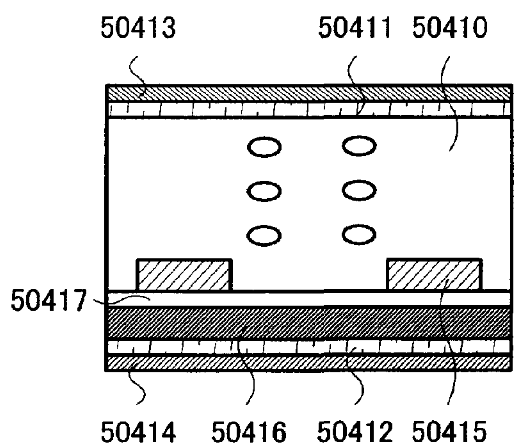

FIG. 43

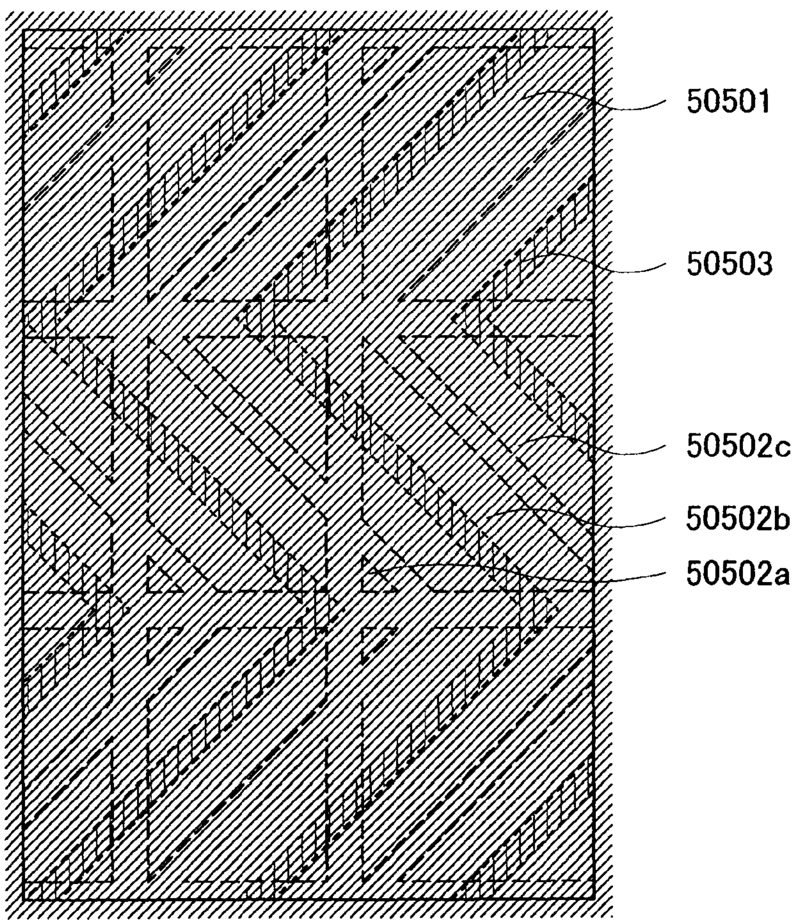

FIG. 44A

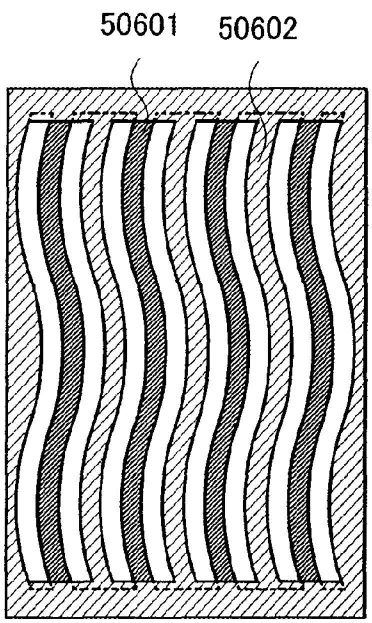

FIG. 44B

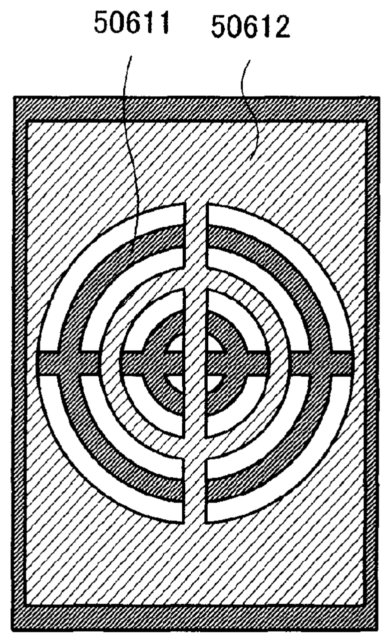

FIG. 44C

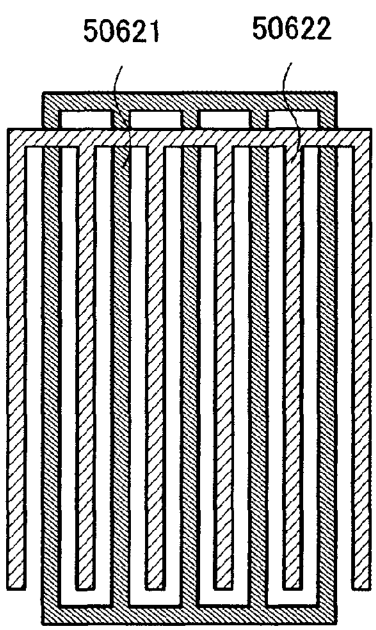

FIG. 44D

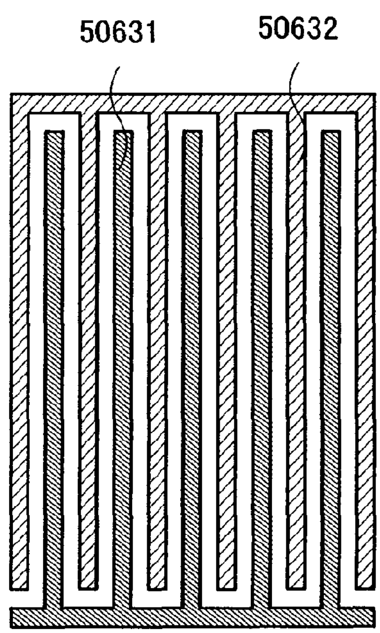

FIG. 45A

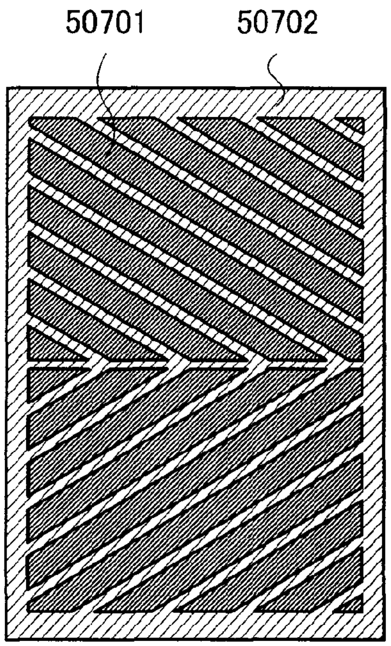

FIG. 45B

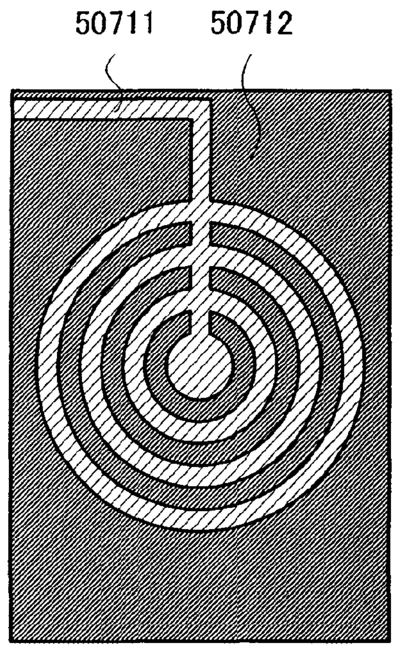

FIG. 45C

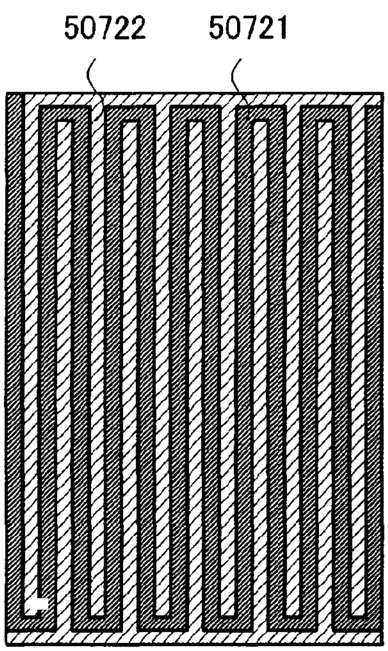

FIG. 45D

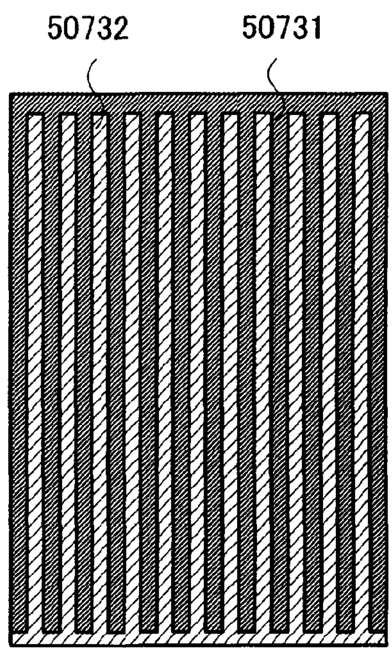

FIG. 46A

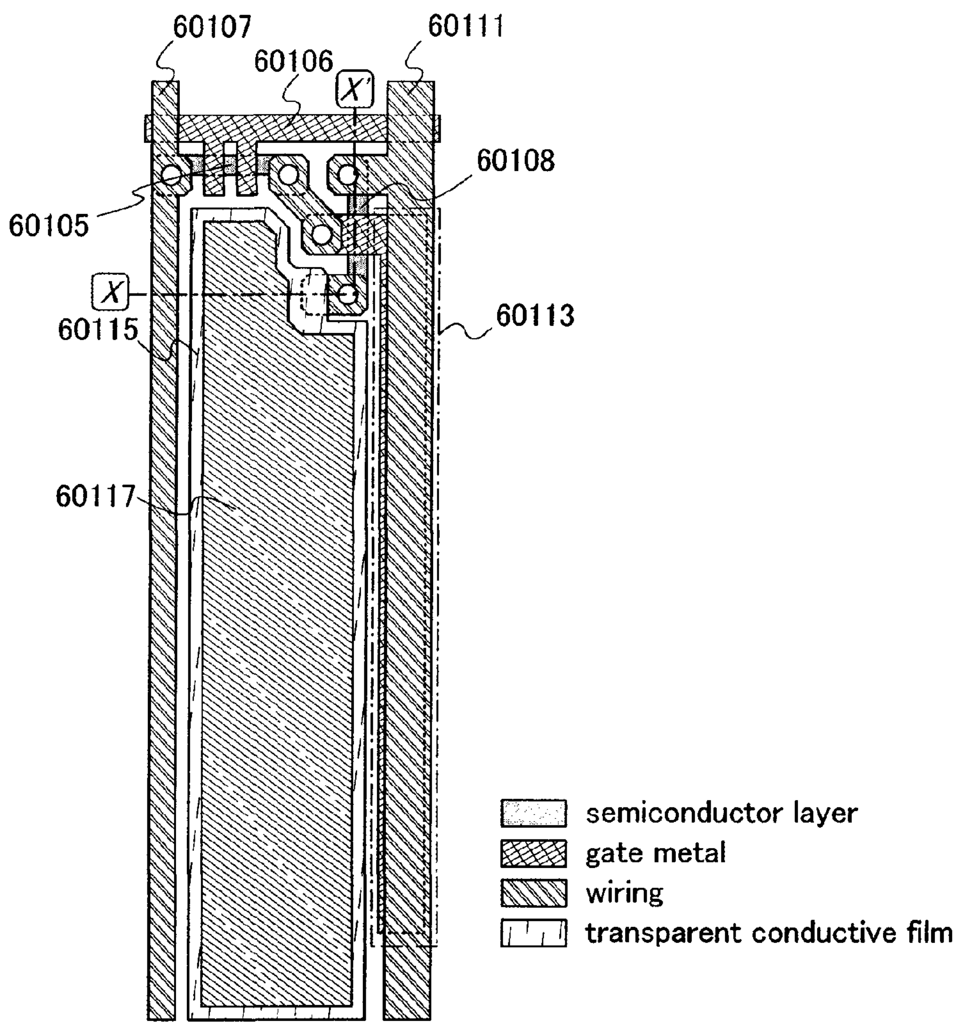

FIG. 46B

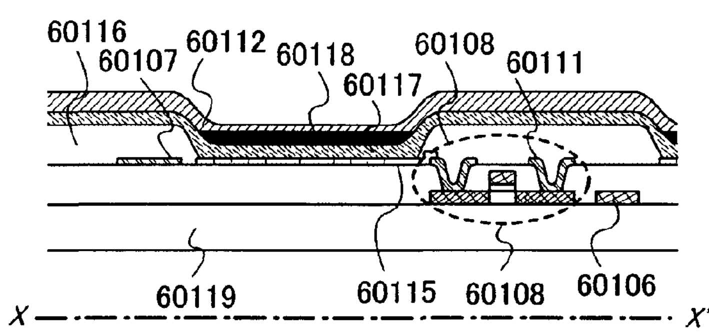

FIG. 47A

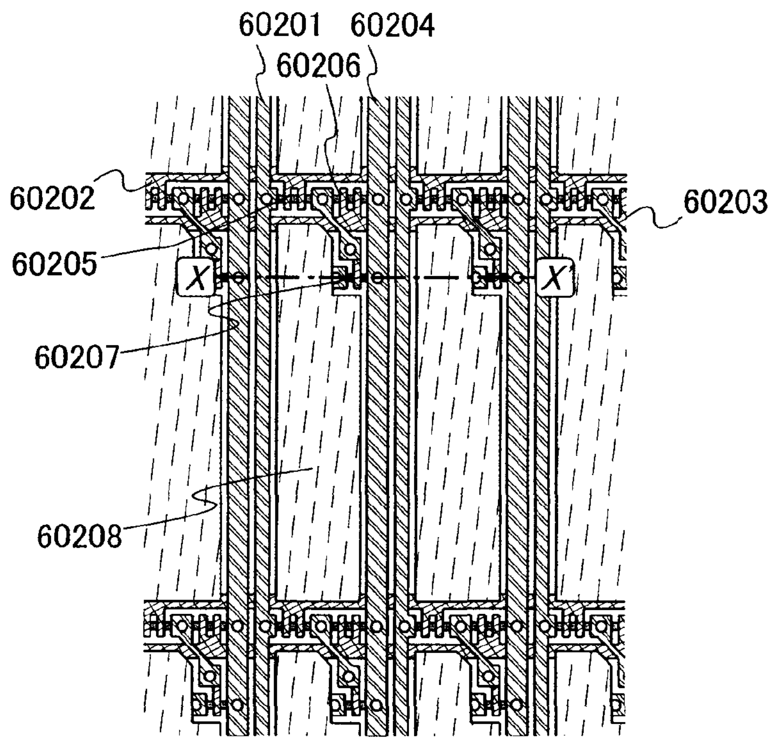

FIG. 47B

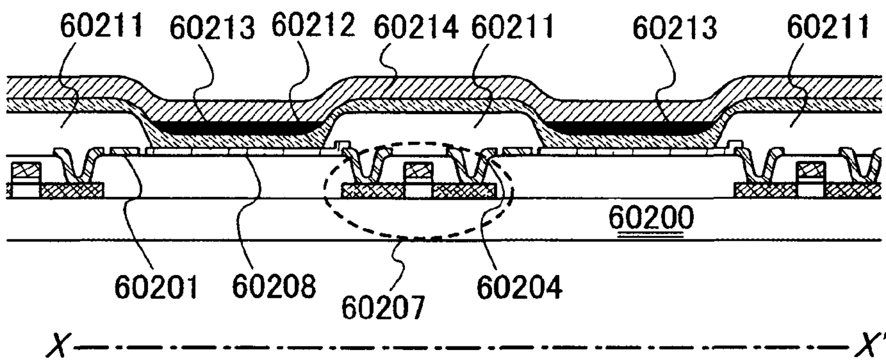

FIG. 48A

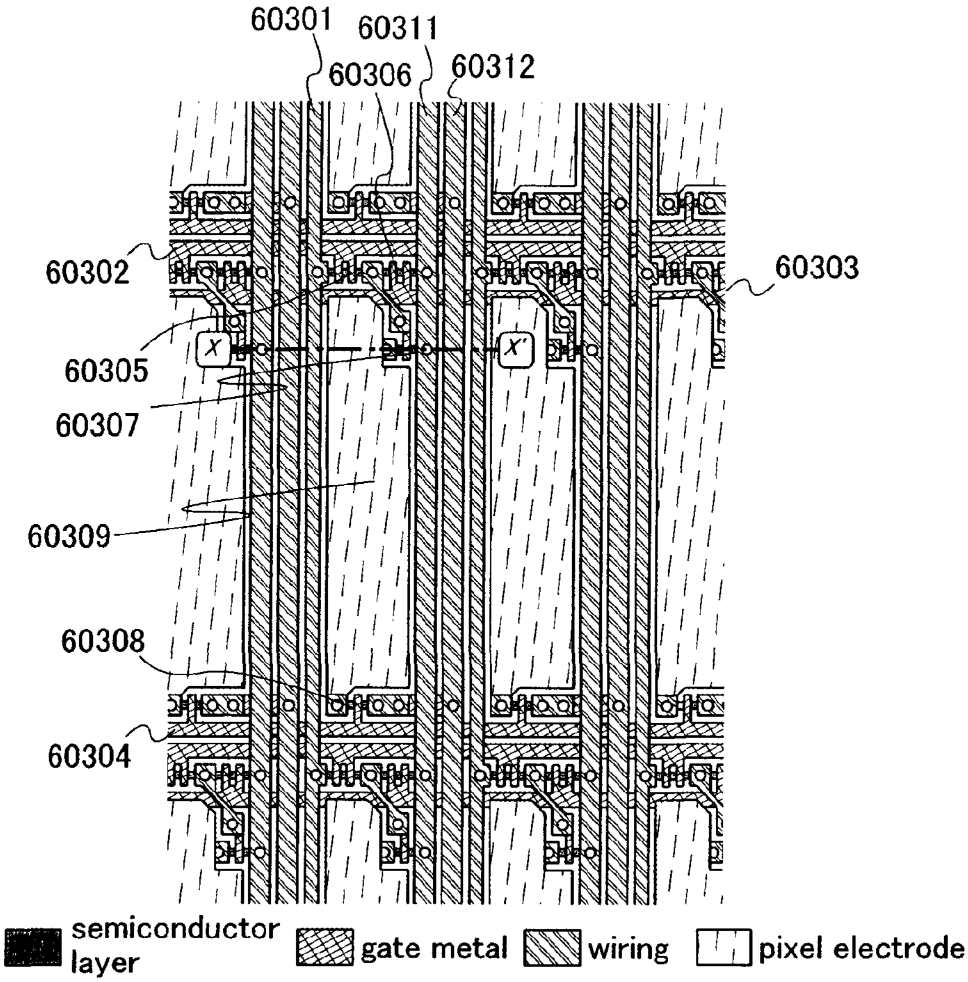

FIG. 48B

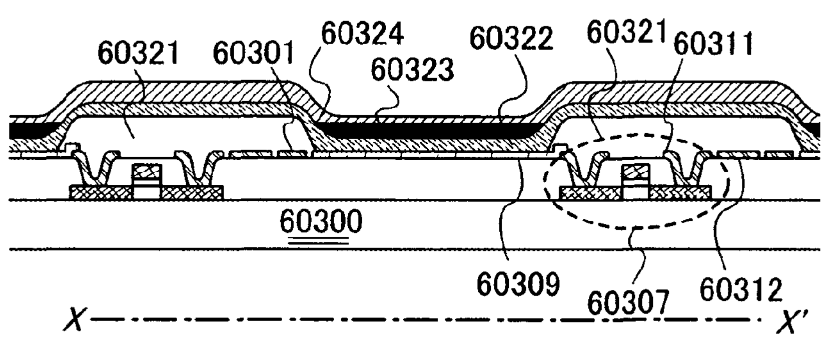

FIG. 49A

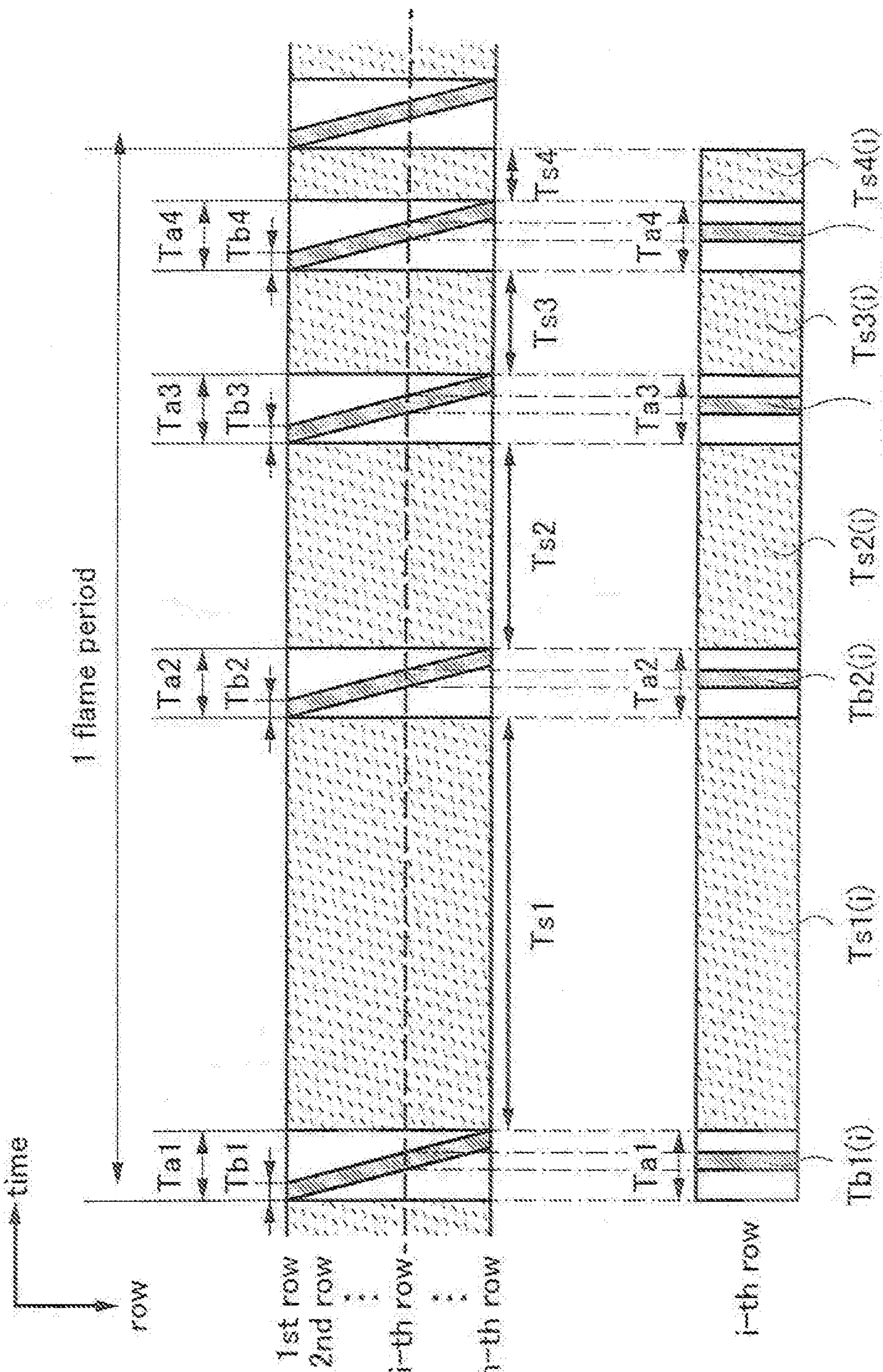

FIG. 49B

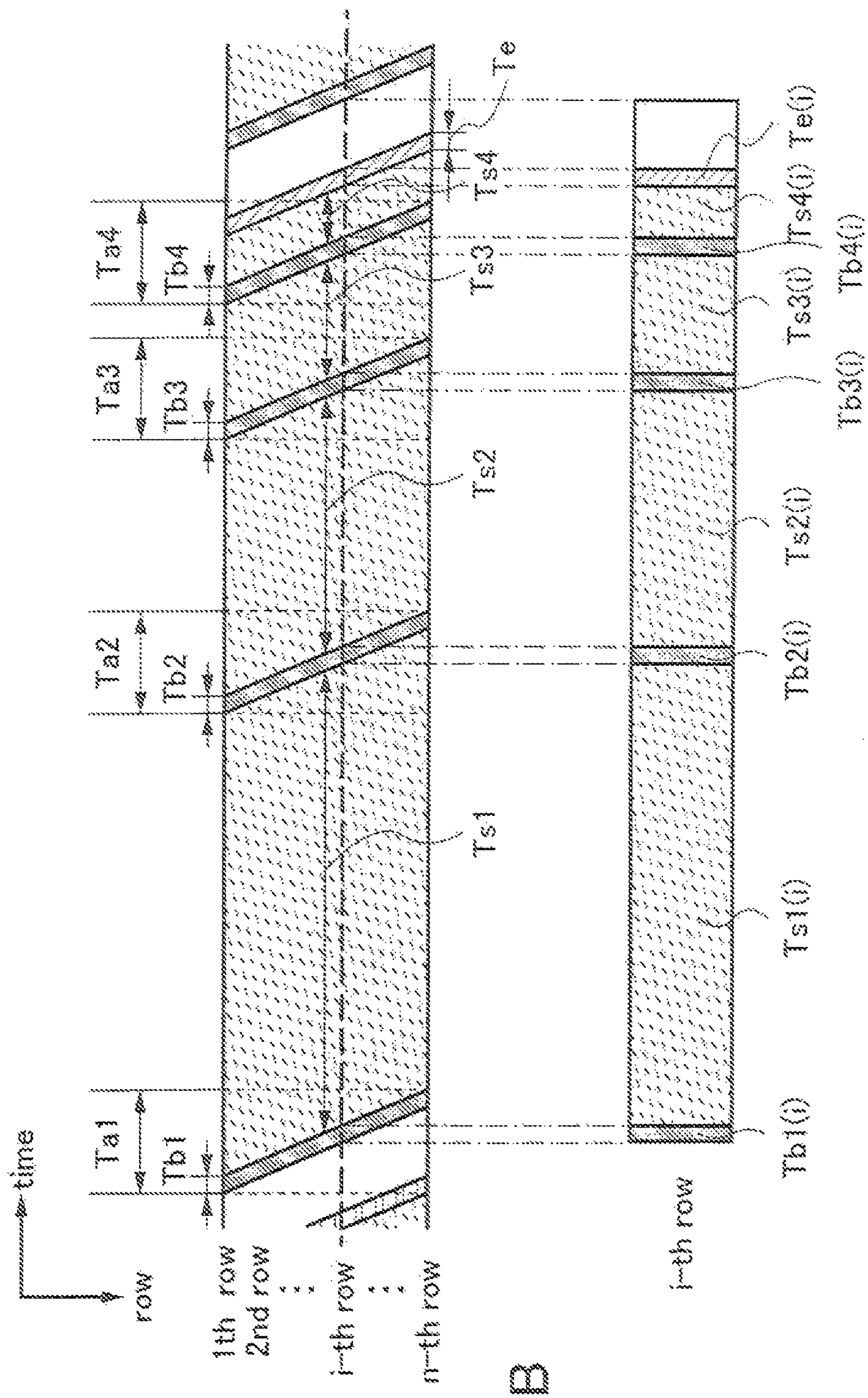

FIG. 50A

FIG. 50B

FIG. 51

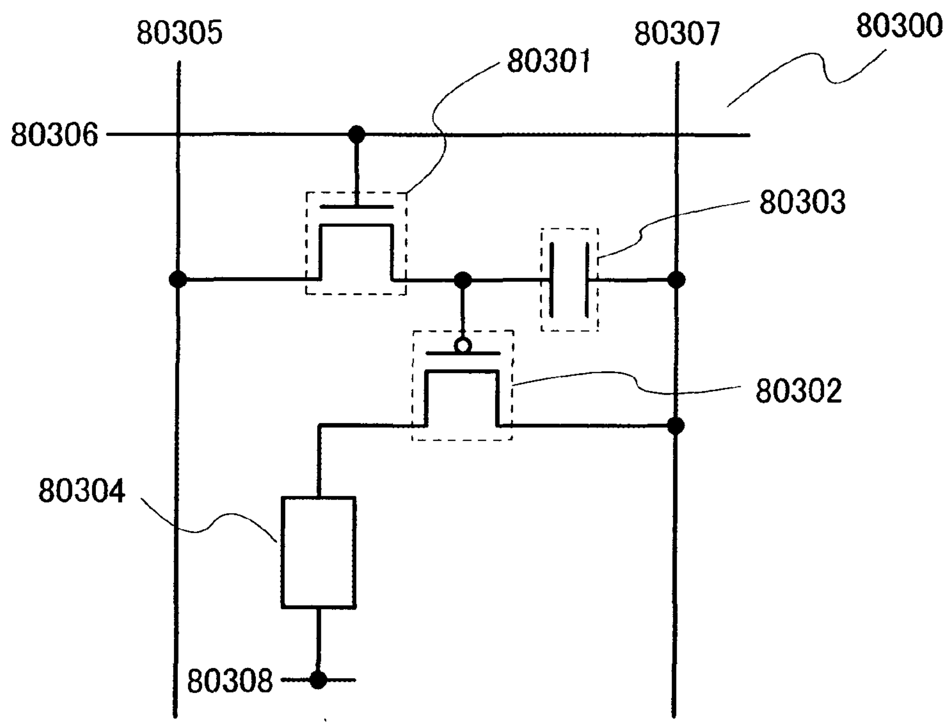

FIG. 52

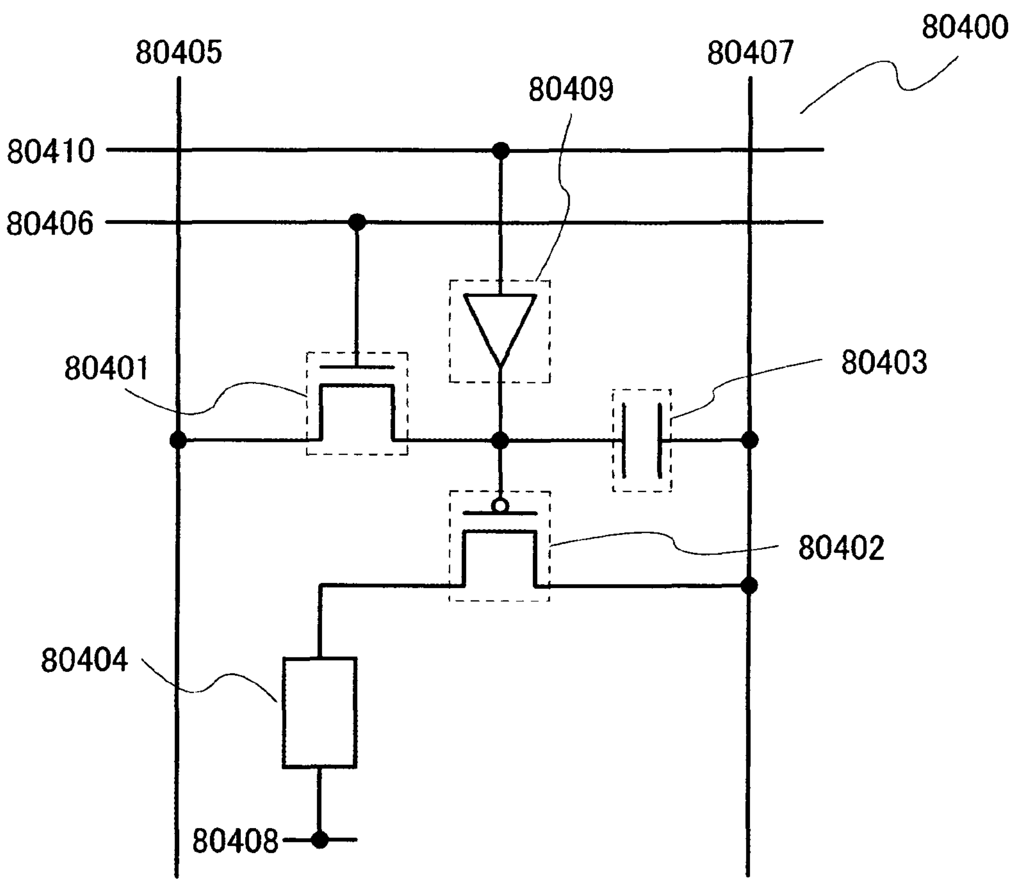
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FIG. 53

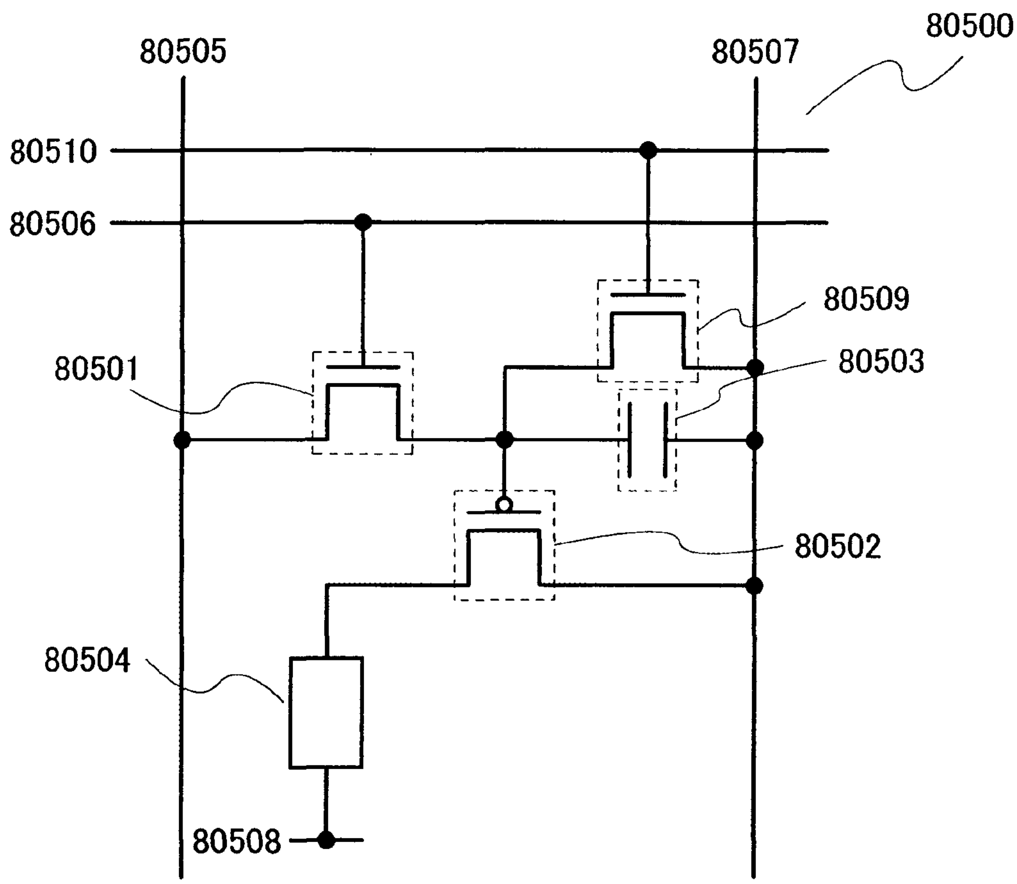
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FIG. 54

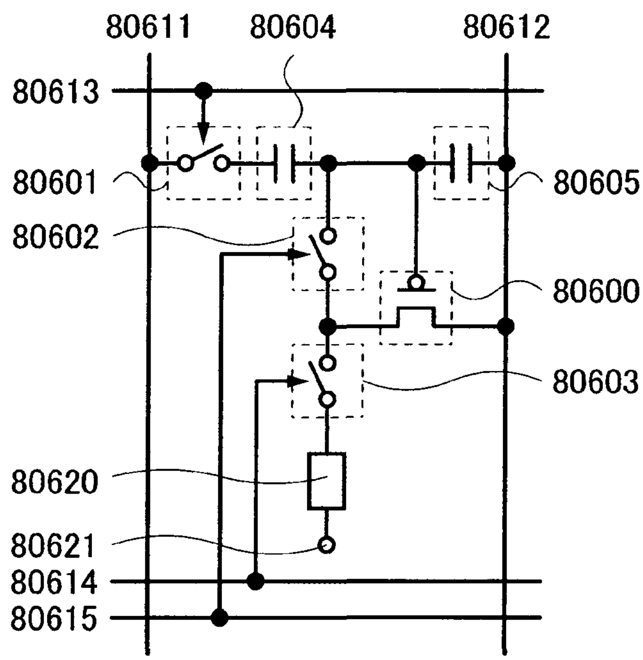
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FIG. 55

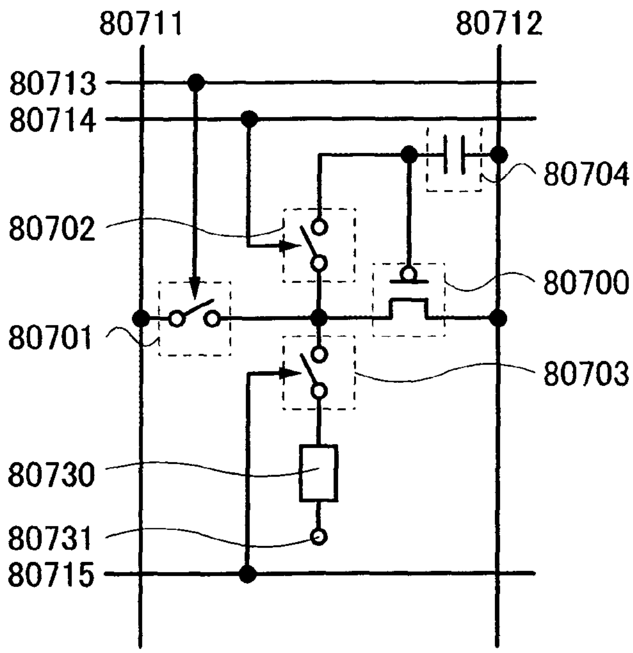

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FIG. 56A

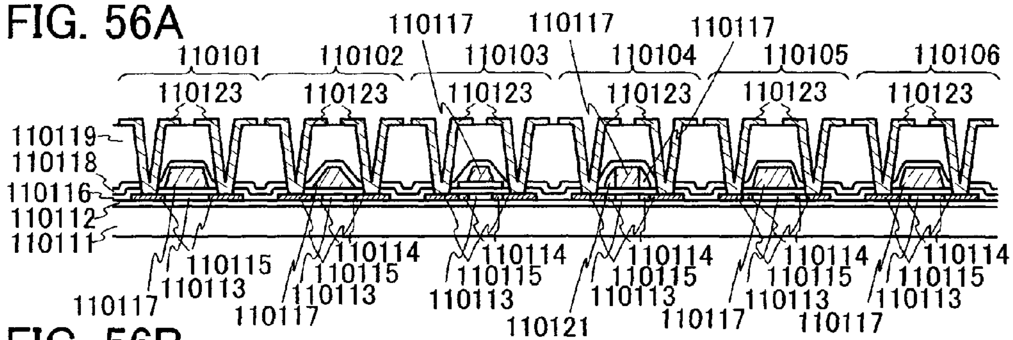

FIG. 56B

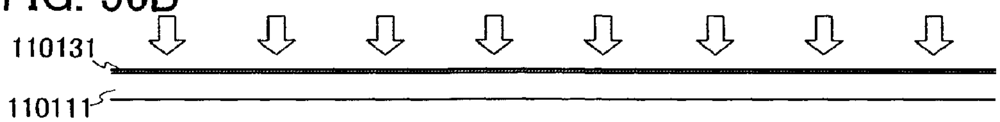

FIG. 56C

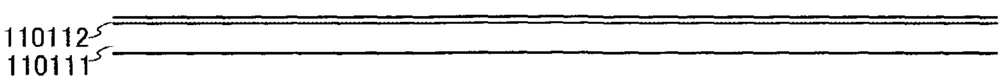

FIG. 56D

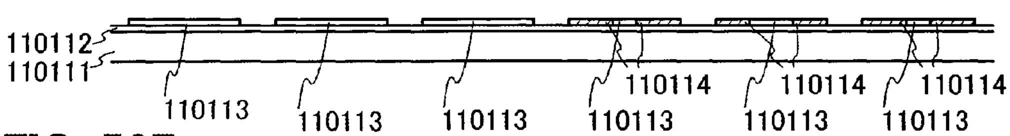

FIG. 56E

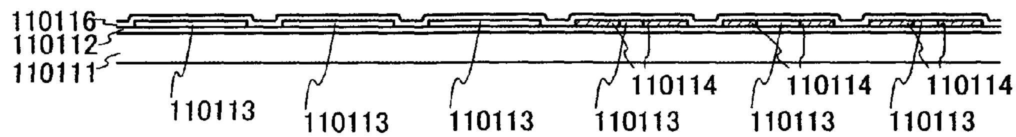

FIG. 56F

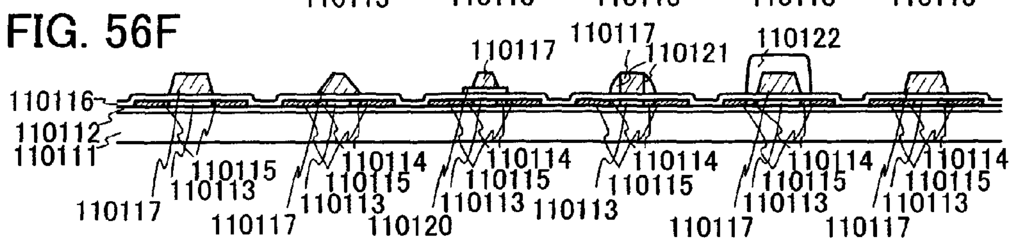

FIG. 56G

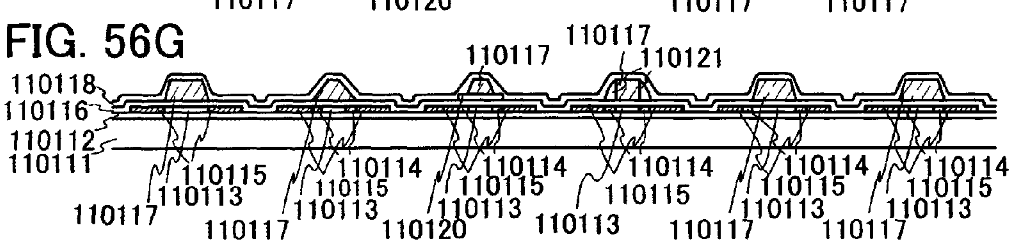

FIG. 57

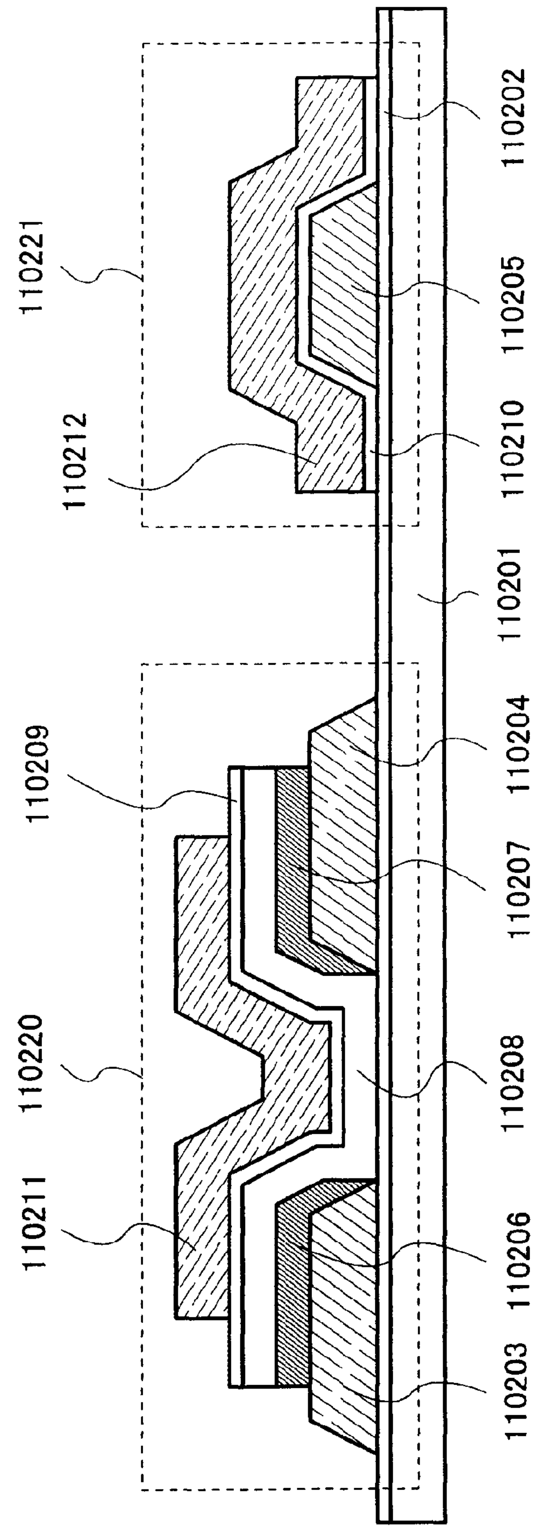
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FIG. 58

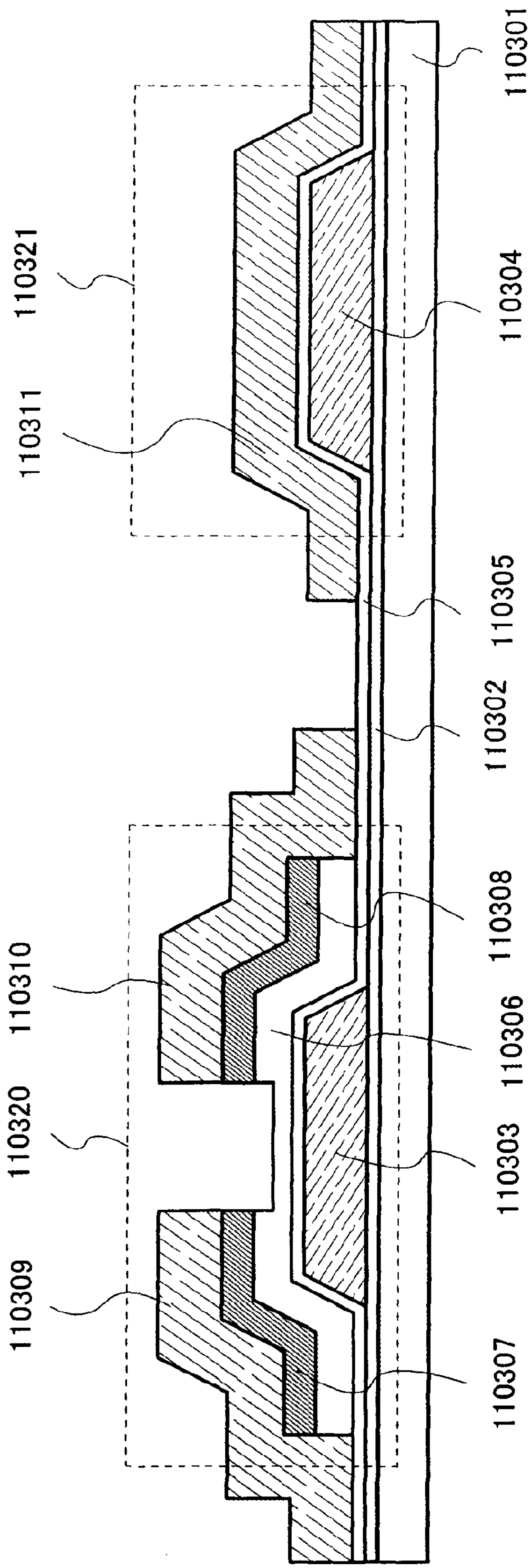
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FIG. 59

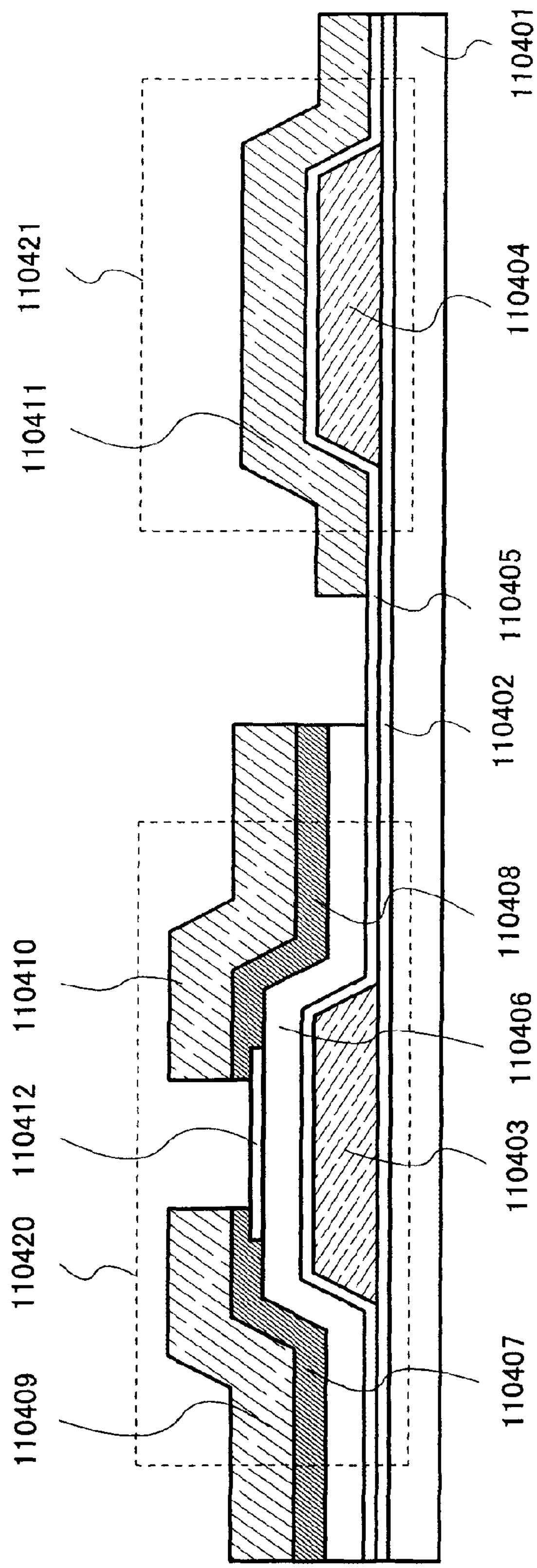
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FIG. 60

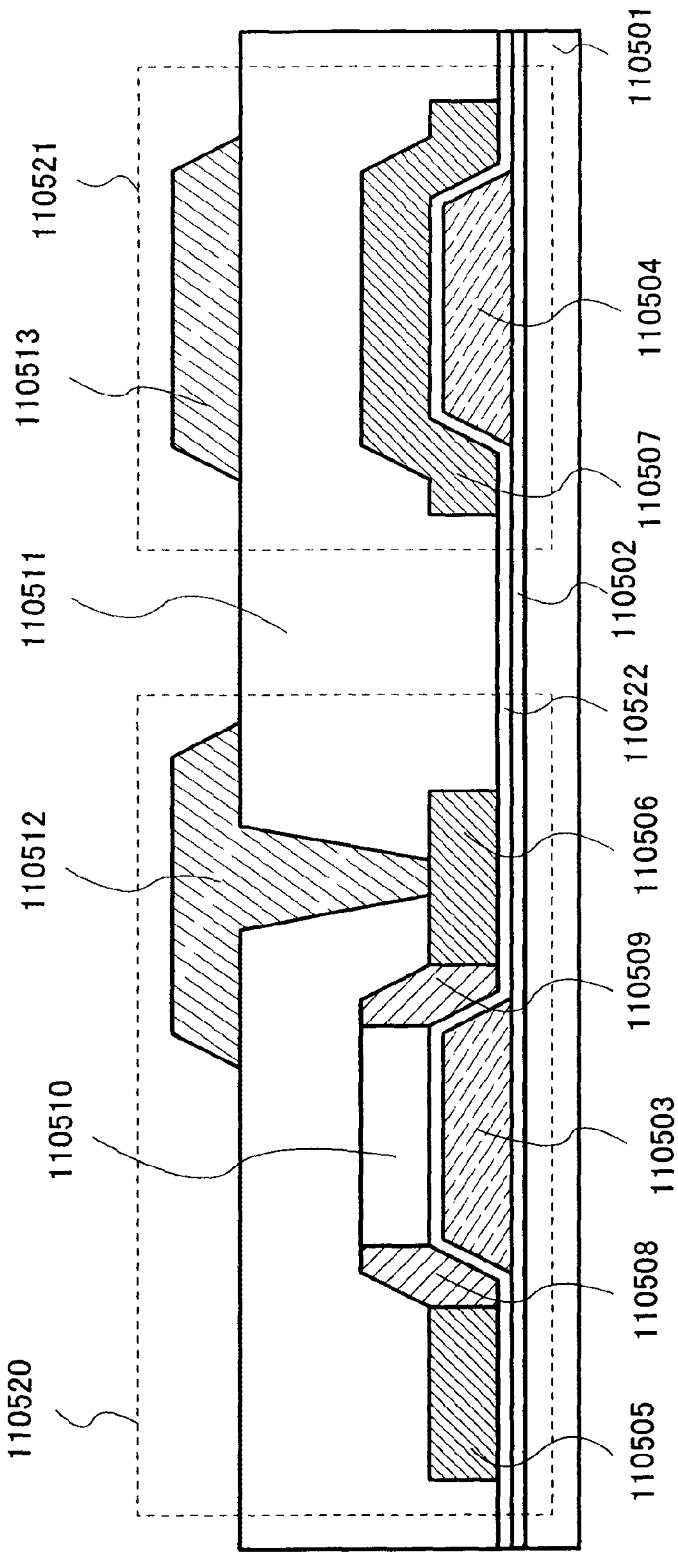
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FIG. 61A

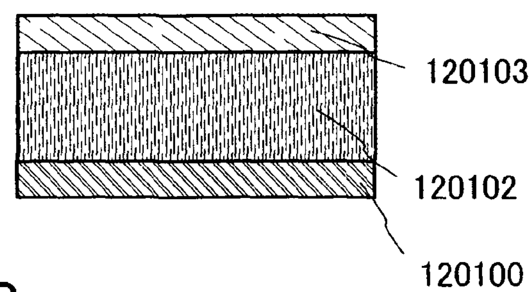


FIG. 61B

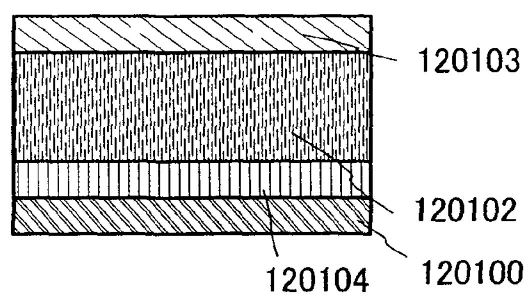


FIG. 61C

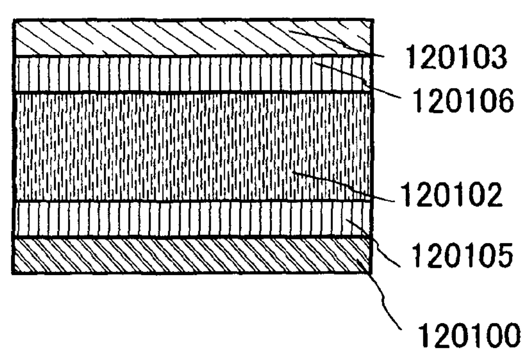


FIG. 62A

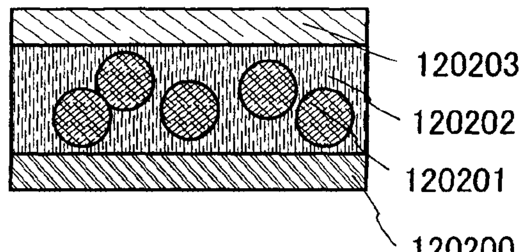


FIG. 62B

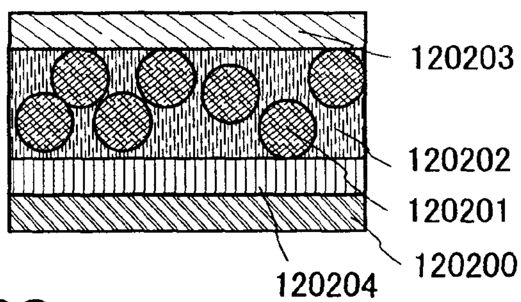


FIG. 62C

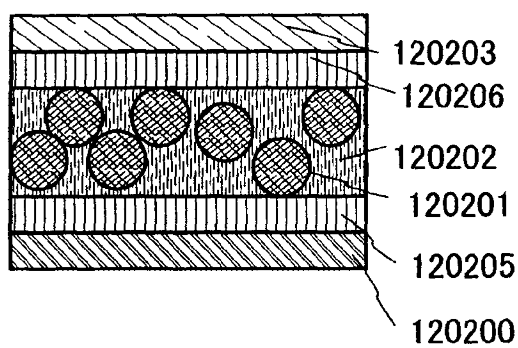


FIG. 63A

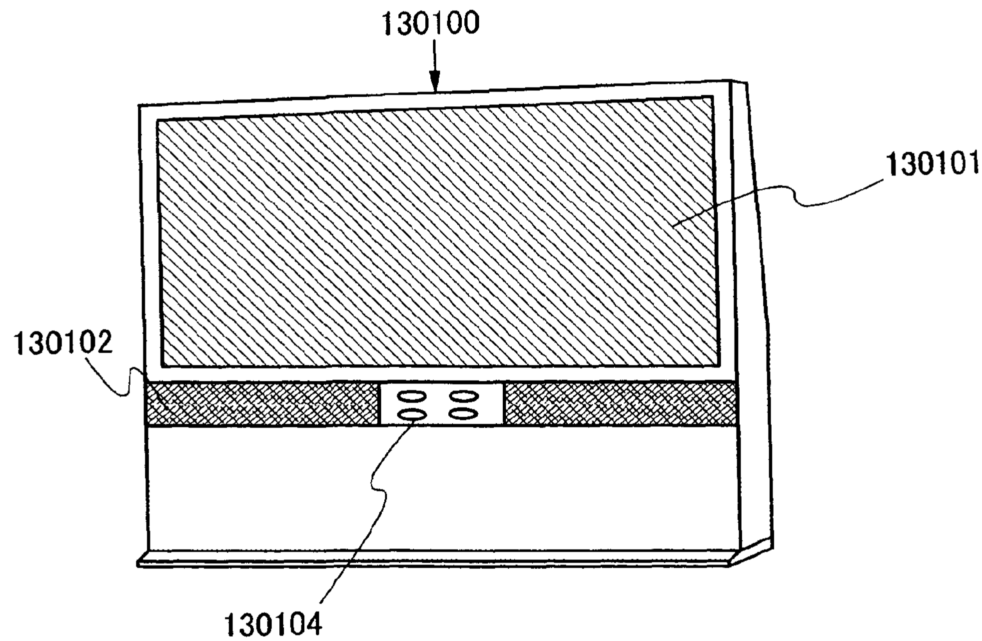


FIG. 63B

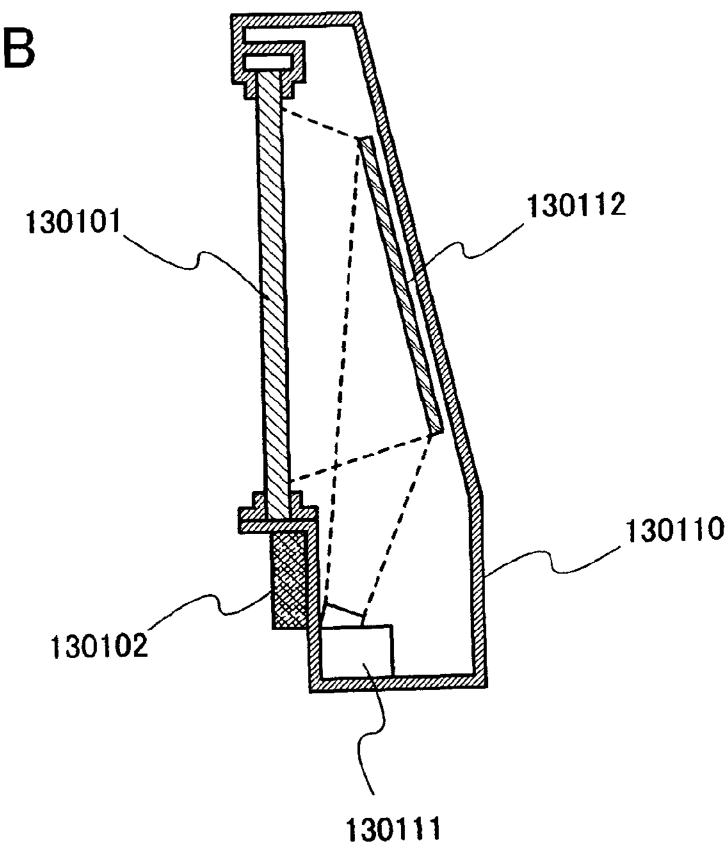


FIG. 64

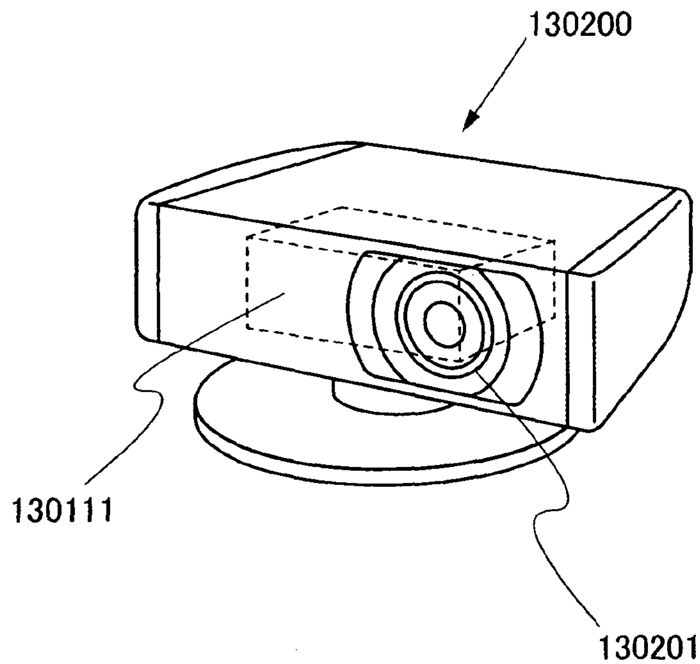


FIG. 65

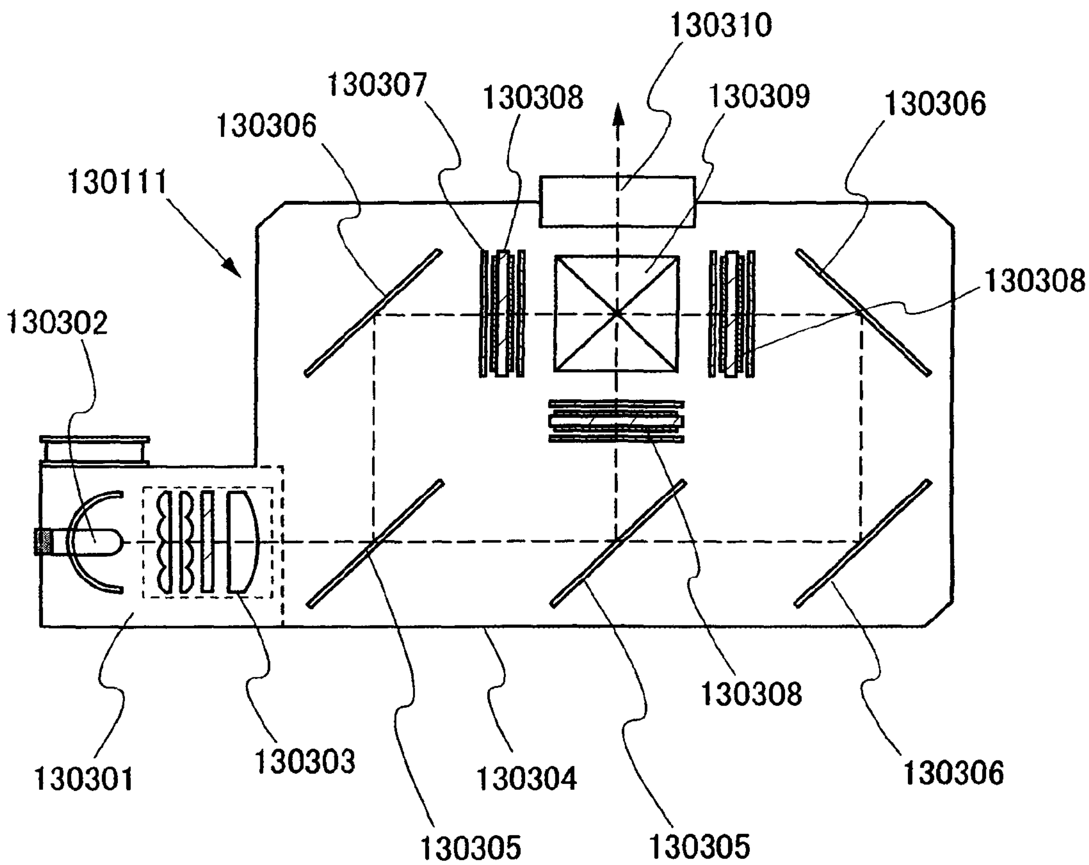

130310
130307
130308
130309
130306
130306
130111
130308
130302
130301
130303
130304
130308
130306
130305
130305

FIG. 66

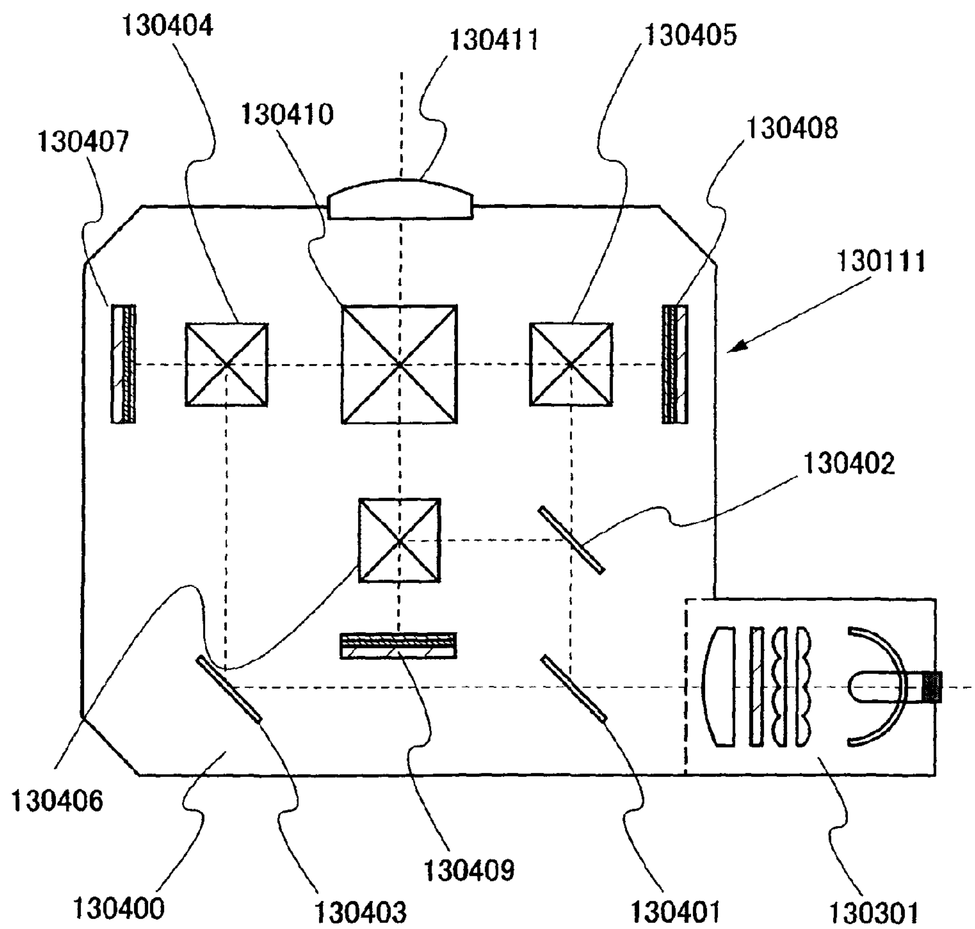

130404
130411
130405
130410
130407
130408
130111
130402
130406
130400
130403
130409
130401
130301

FIG. 67A

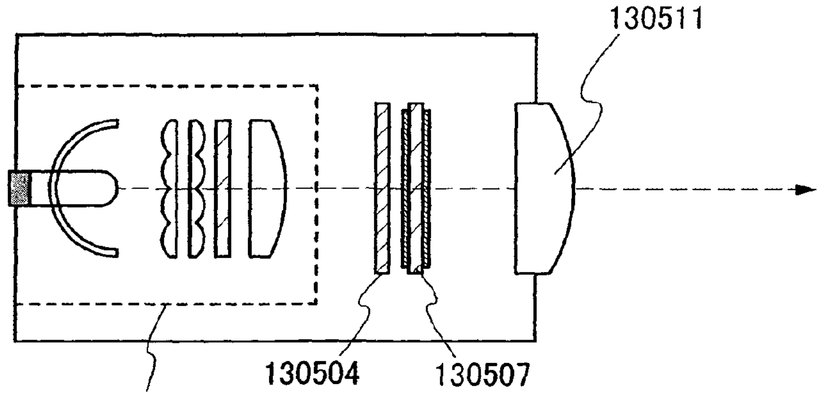


FIG. 67B

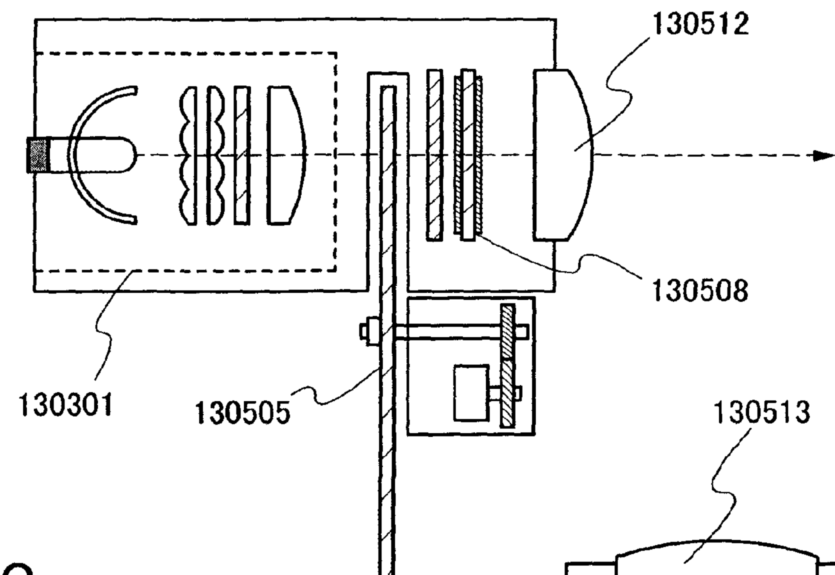


FIG. 67C

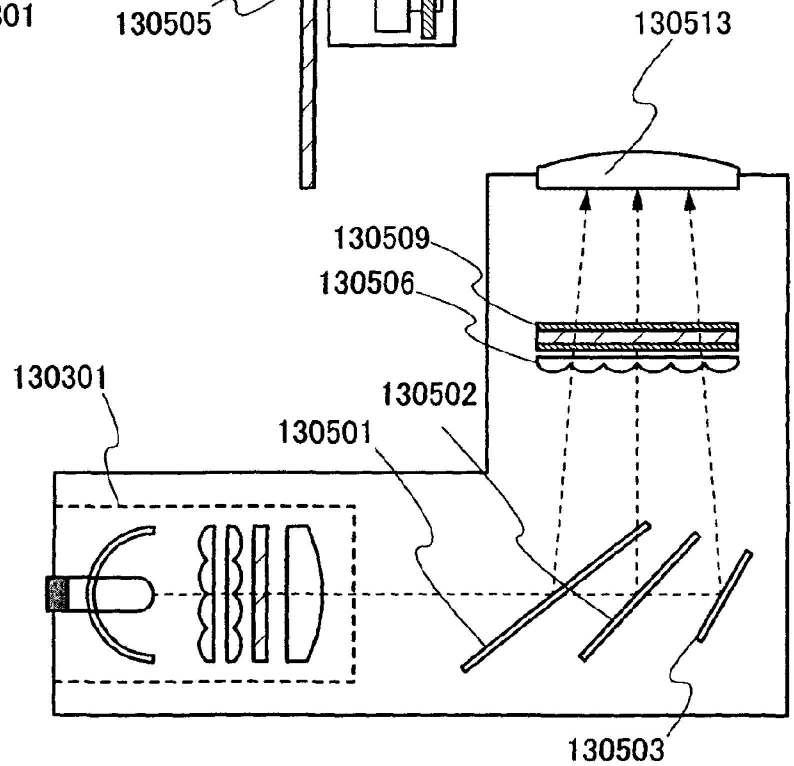


FIG. 68

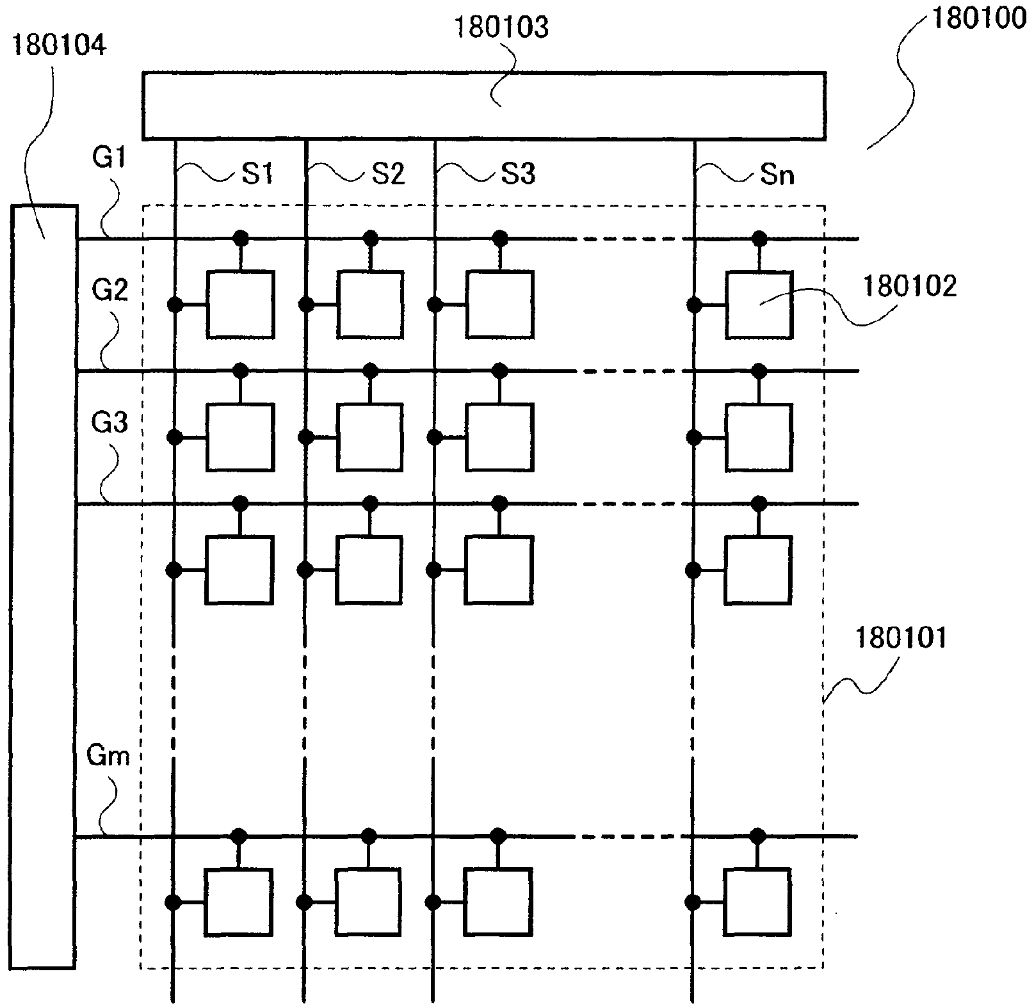


FIG. 69

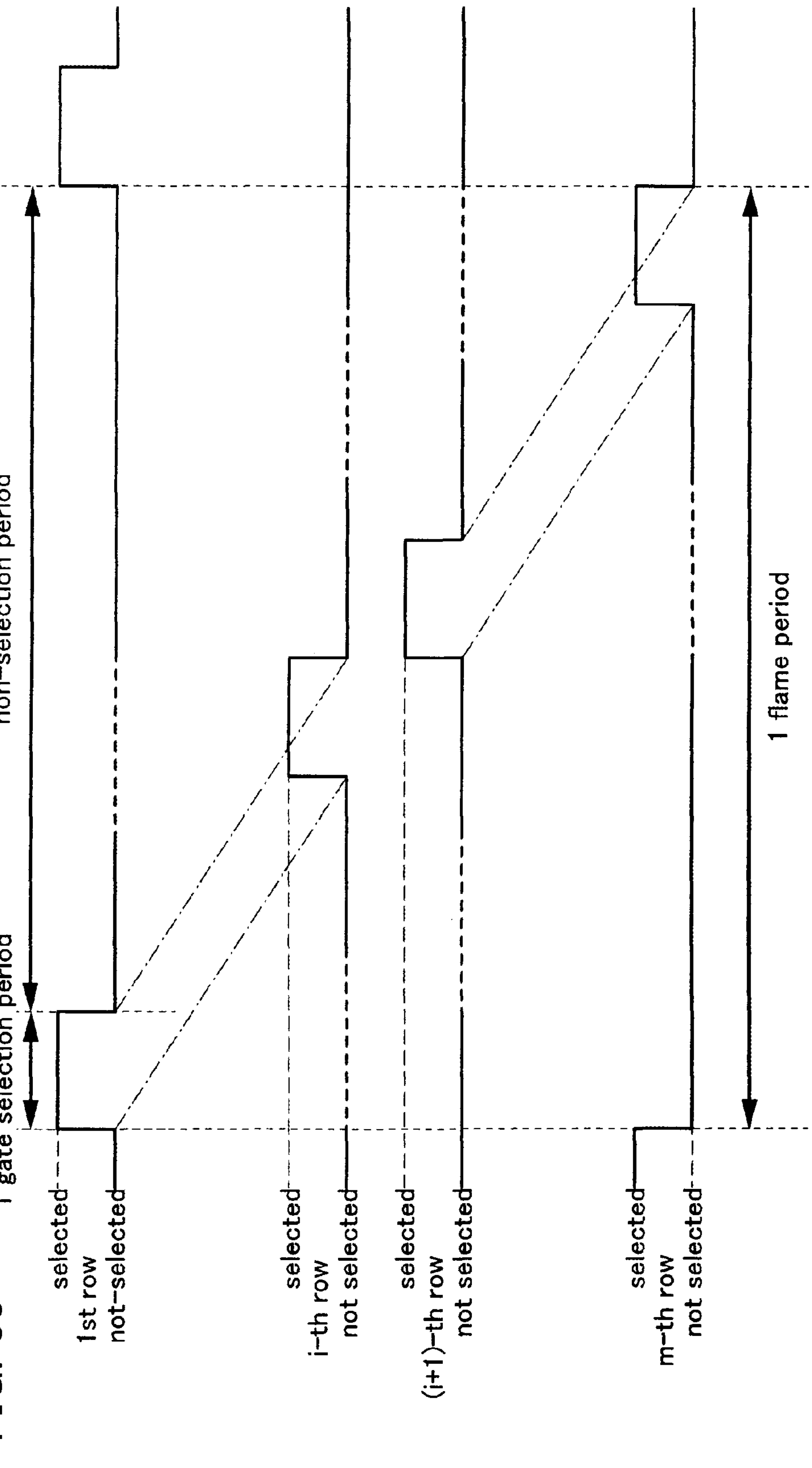

1 gate selection period
non-selection period
1 flame period
1st row
selected
not-selected
i-th row
selected
not selected
(i+1)-th row
selected
not selected
m-th row
selected
not selected

FIG. 70

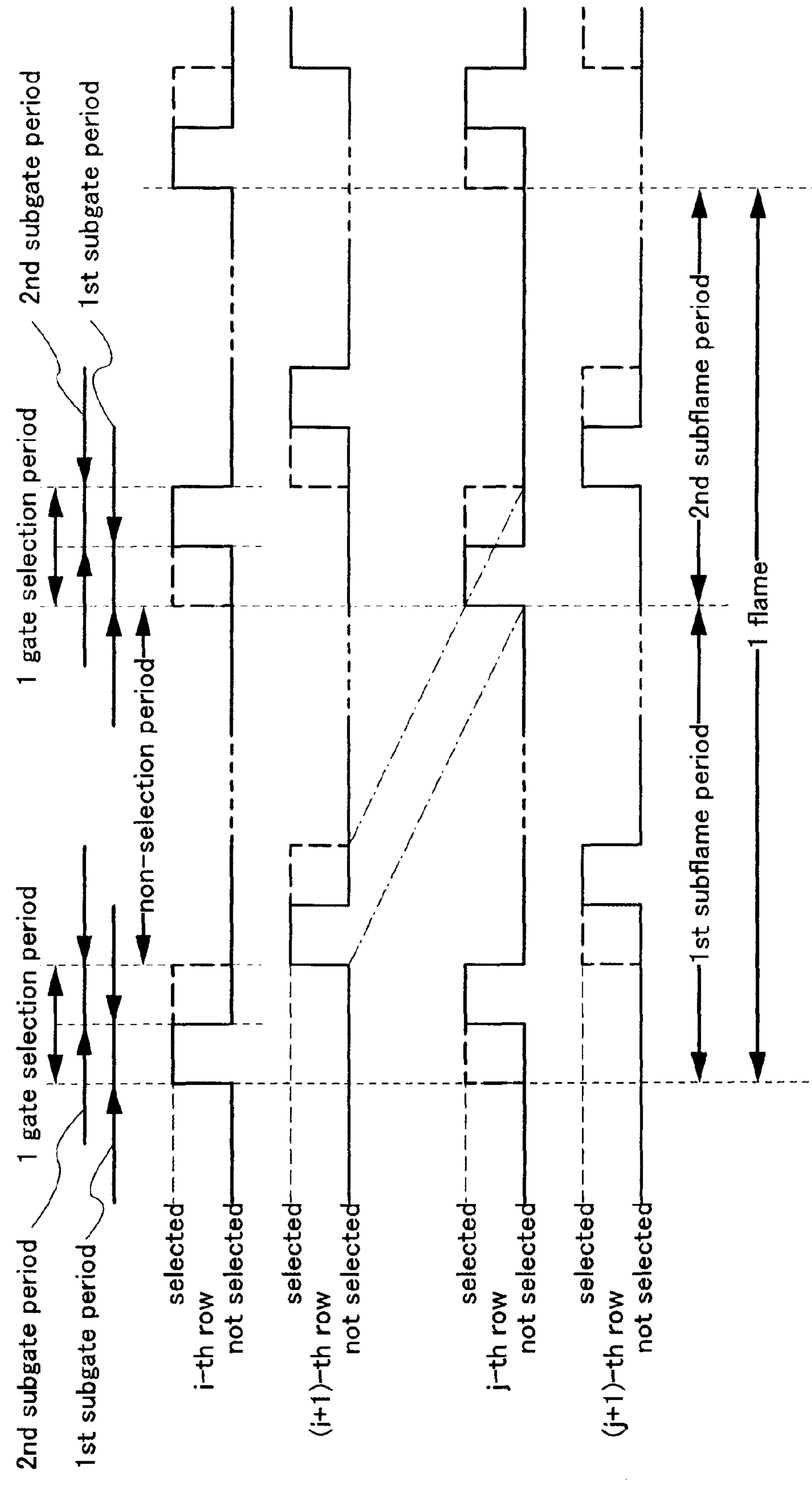

2nd subgate period
1st subgate period
1 gate selection period
1 gate selection period
2nd subgate period
1st subgate period
non-selection period
selected
i-th row
not selected
selected
(i+1)-th row
not selected
selected
j-th row
not selected
selected
(j+1)-th row
not selected
1st subflame period
2nd subflame period
1 flame

FIG. 71A

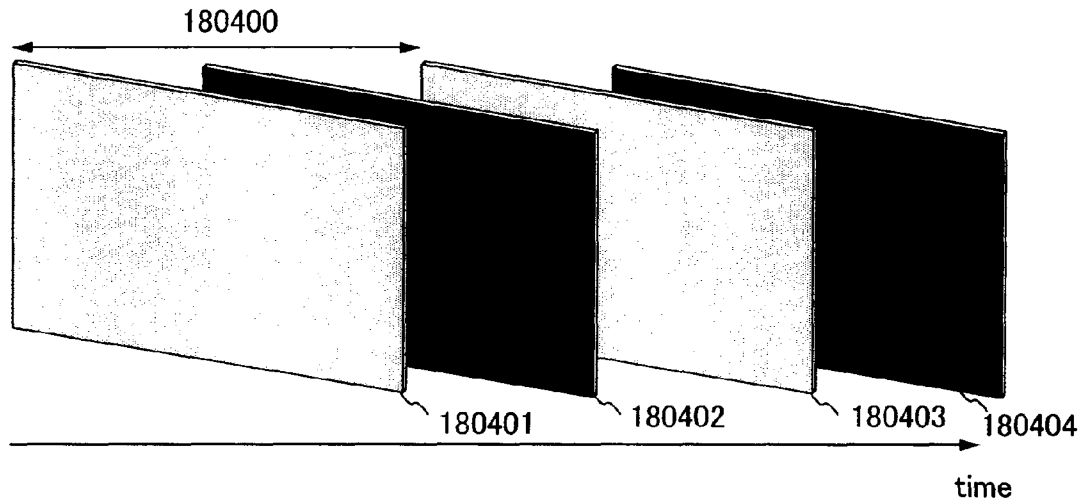


FIG. 71B

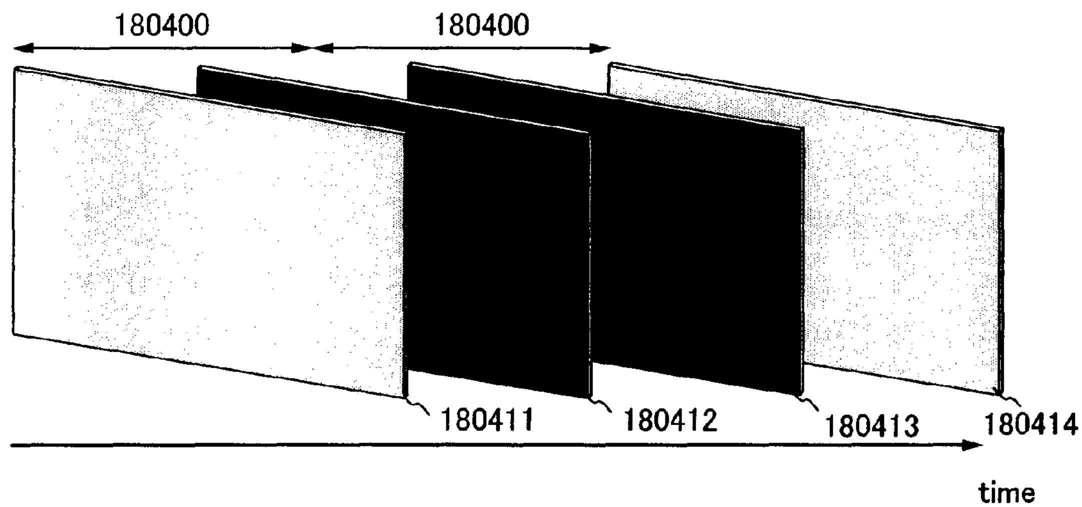


FIG. 72A

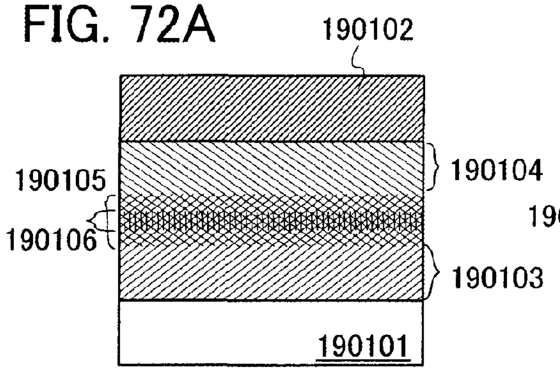


FIG. 72B

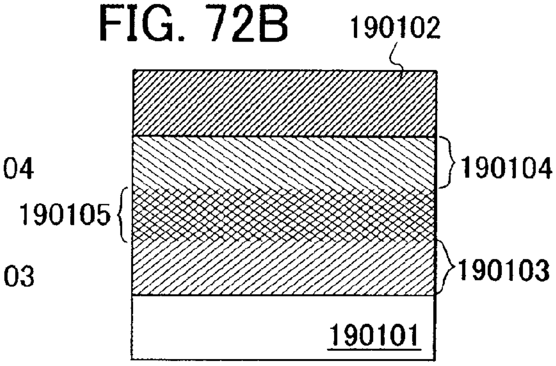


FIG. 72C

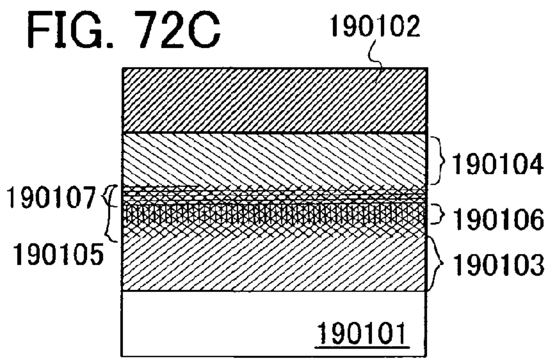


FIG. 72D

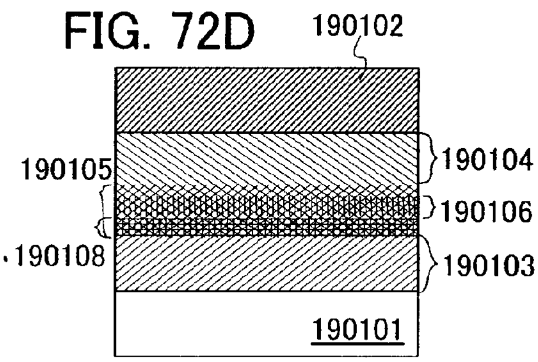


FIG. 72E

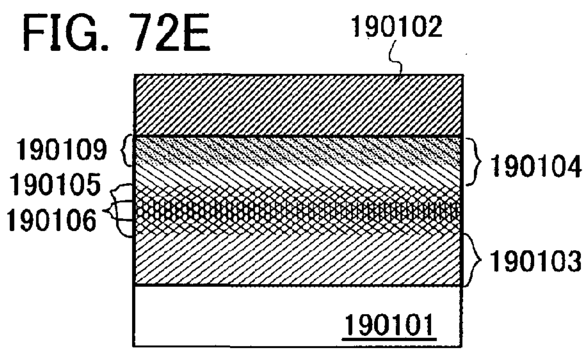


FIG. 73

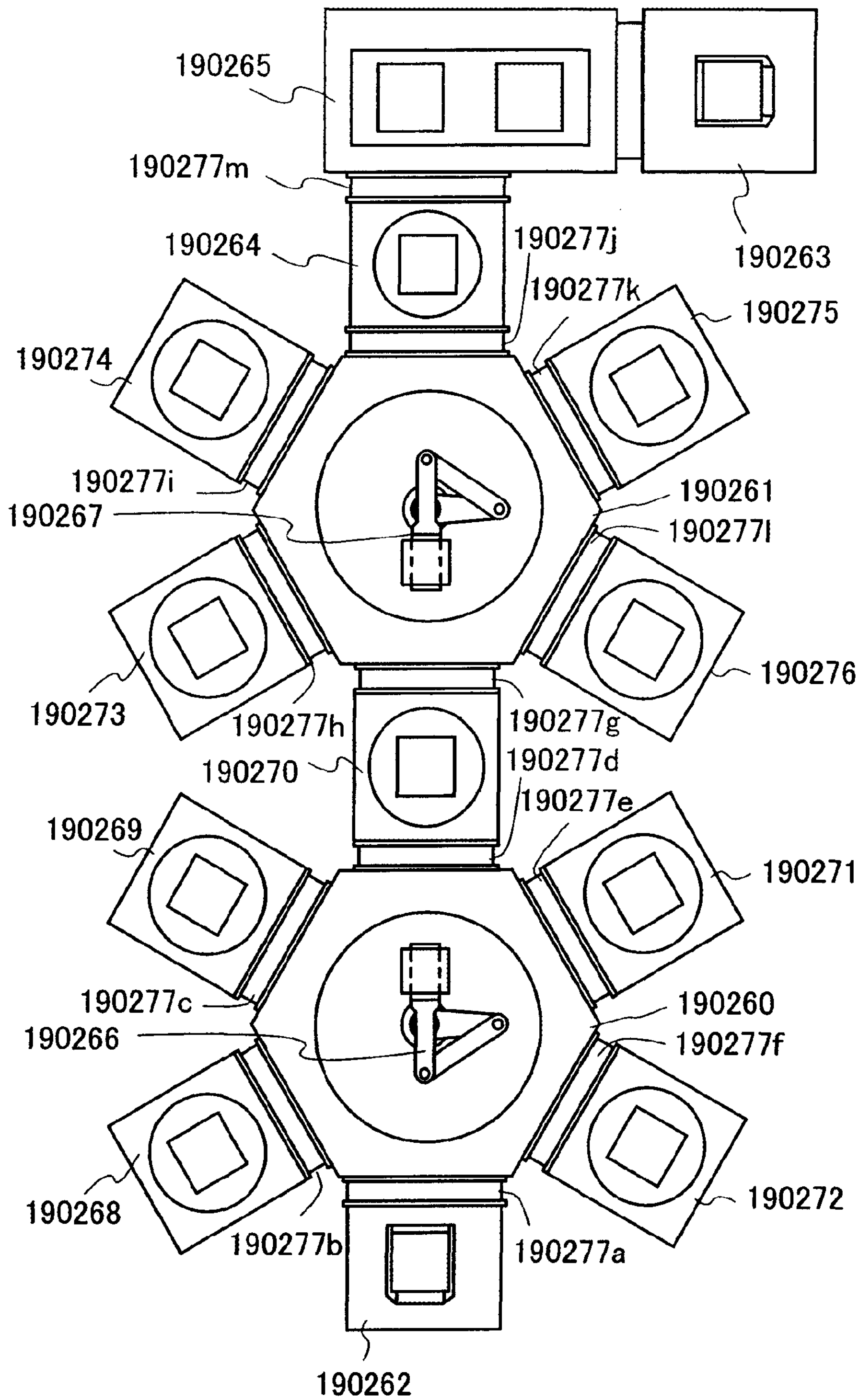

190265
190263
190277m
190264
190277j
190277k
190275
190274
190277i
190261
190267
190277l
190276
190273
190277h
190277g
190270
190277d
190277e
190269
190271
190277c
190260
190266
190277f
190268
190272
190277b
190277a
190262

FIG. 74

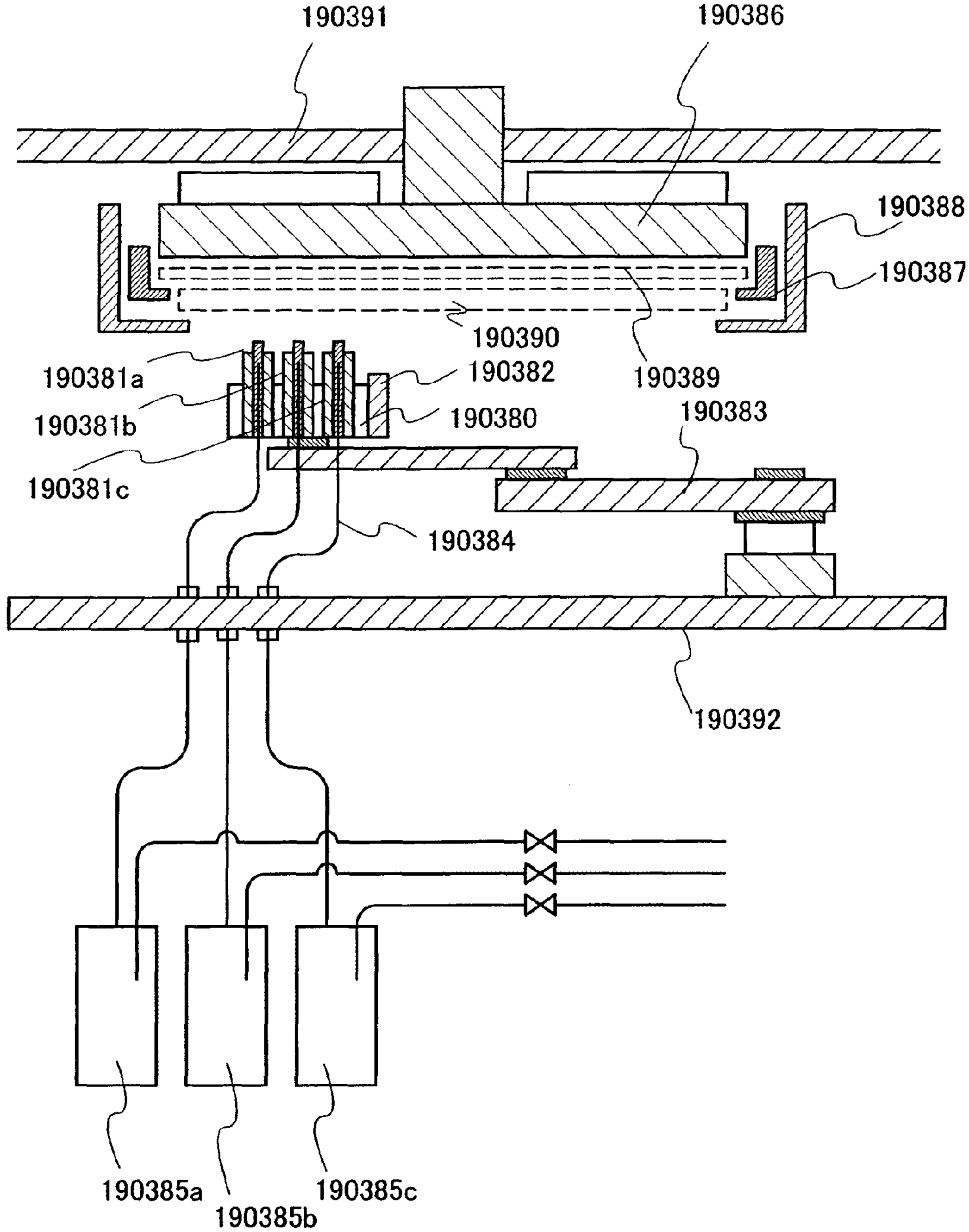

190391
190386
190388
190387
190390
190389
190381a
190382
190381b
190380
190383
190381c
190384
190392
190385a
190385b
190385c

FIG. 75

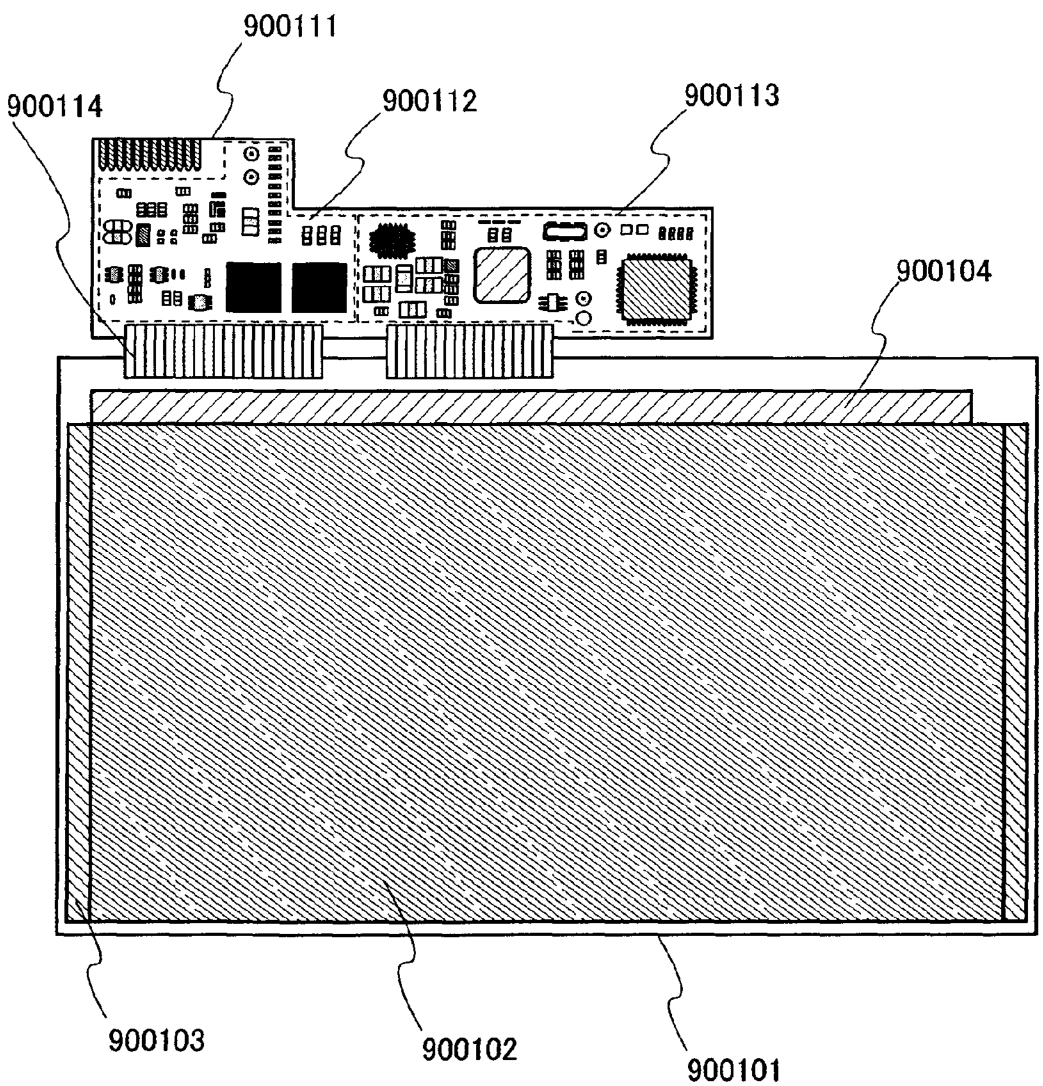


FIG. 76

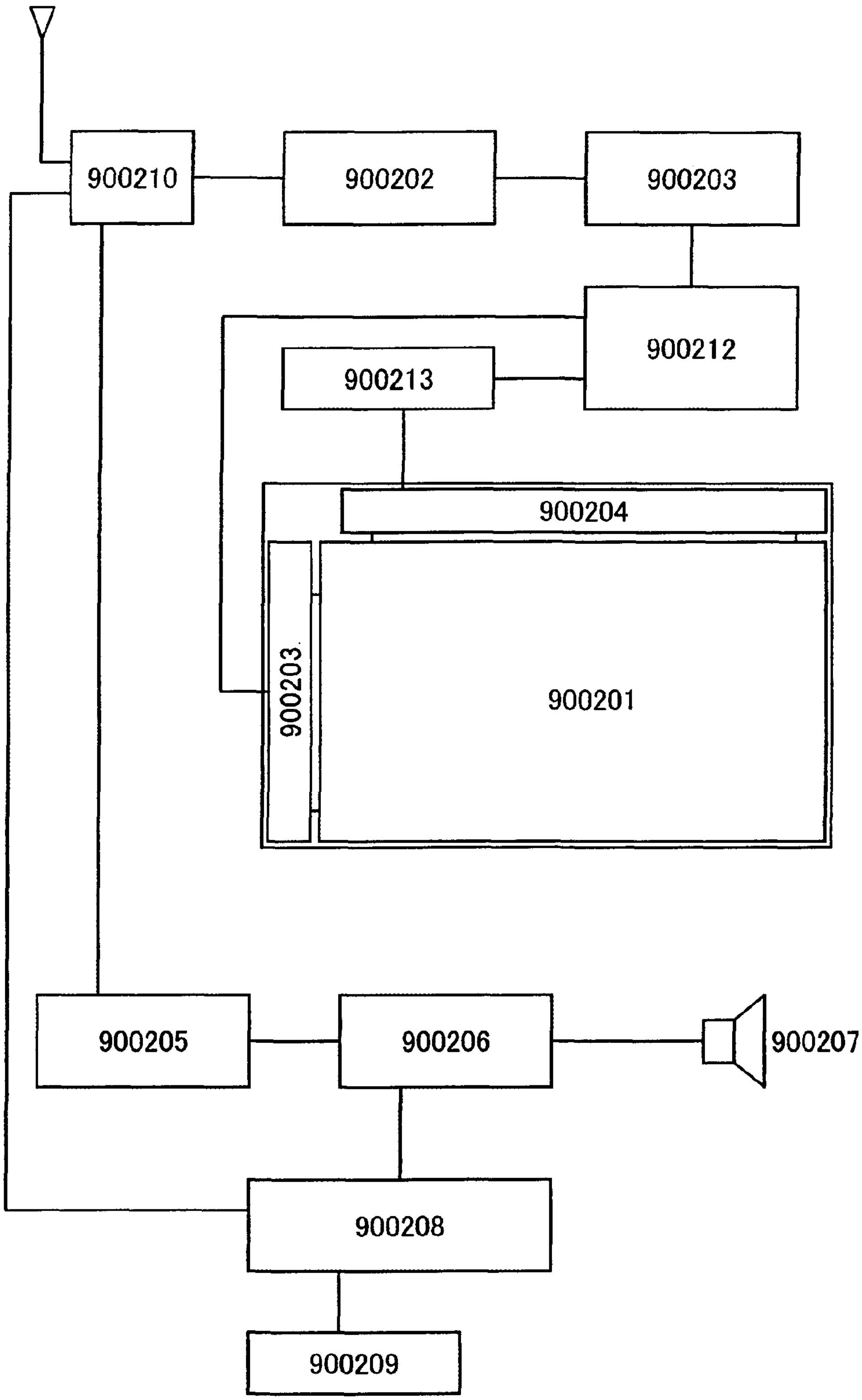

900210
900202
900203
900212
900213
900204
900203
900201
900205
900206
900207
900208
900209

FIG. 77A

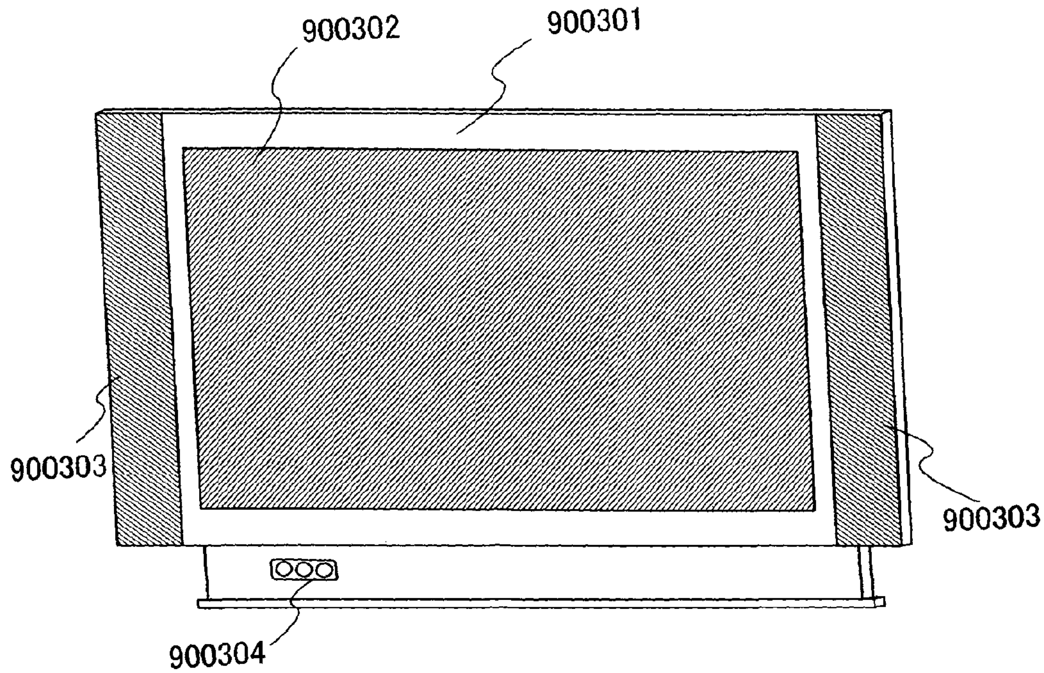


FIG. 77B

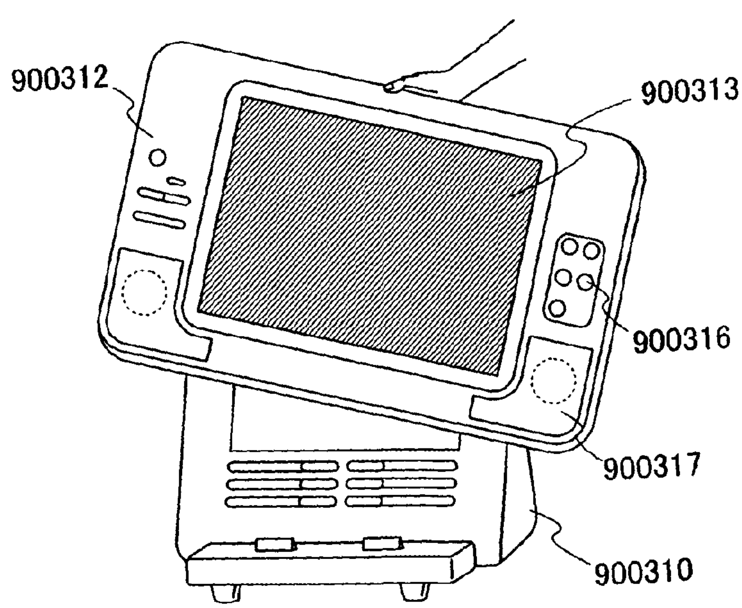


FIG. 78A

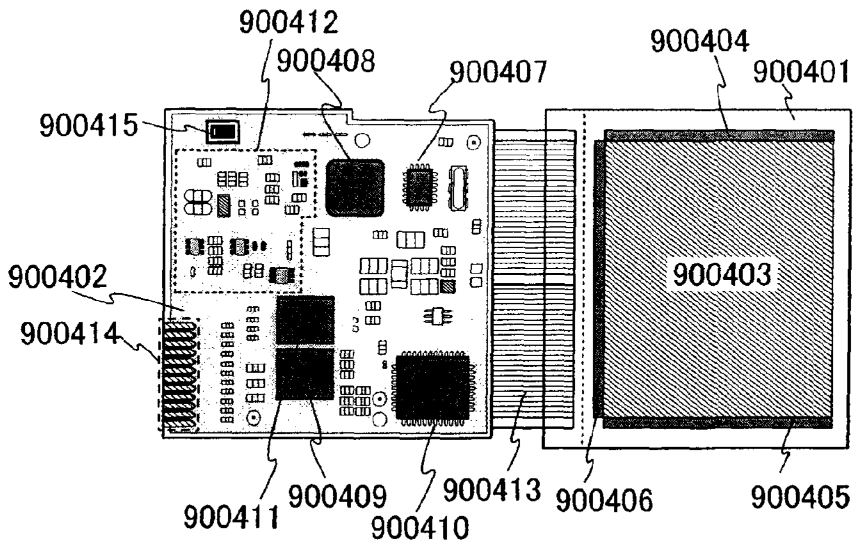


FIG. 78B

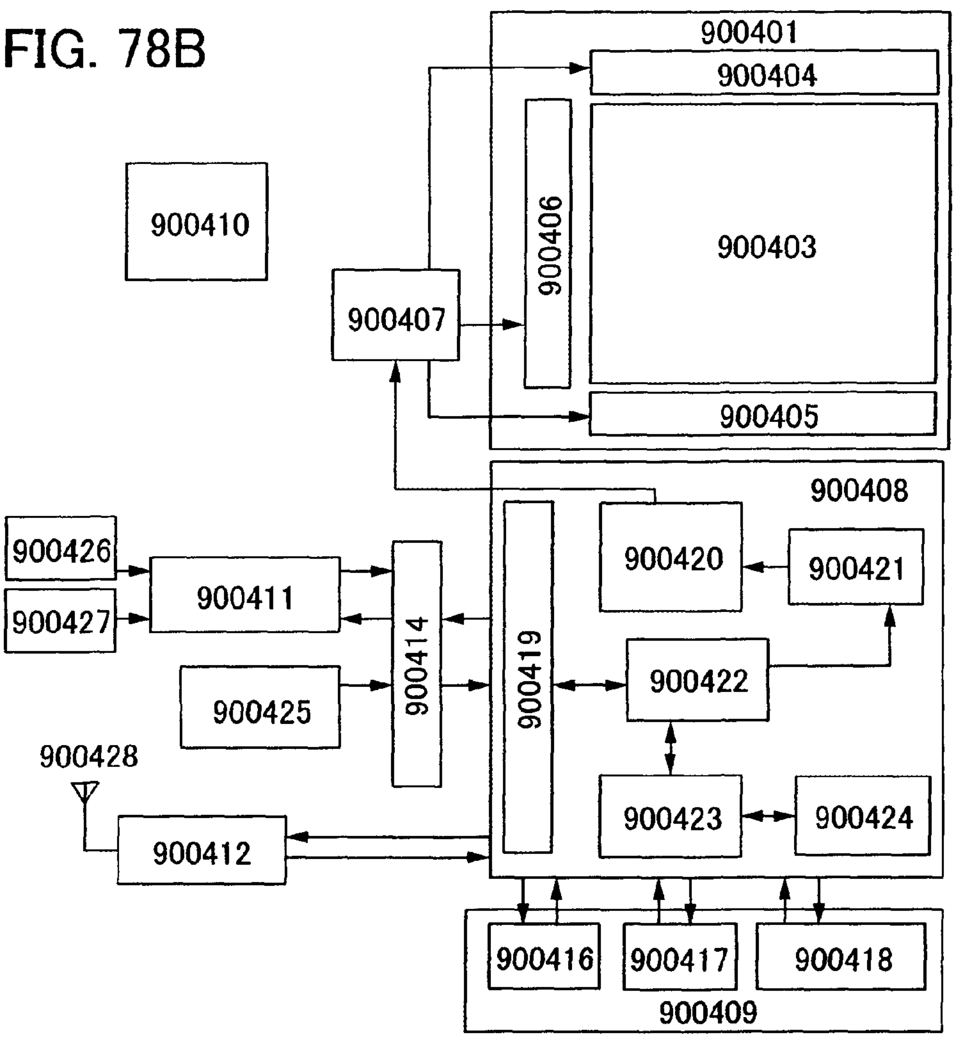
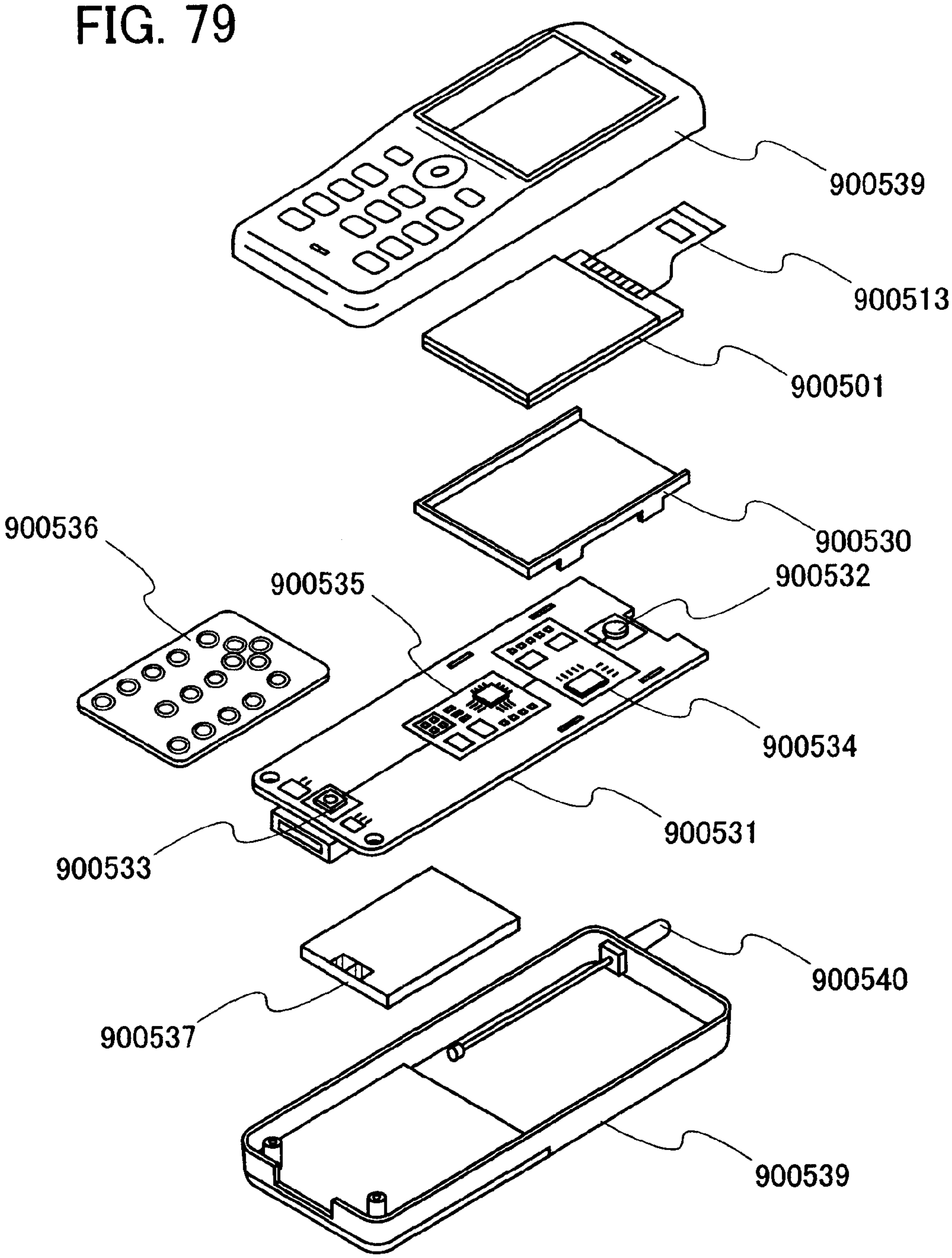


FIG. 79



900539
900513
900501
900530
900536
900535
900532
900534
900531
900533
900540
900537
900539

FIG. 80

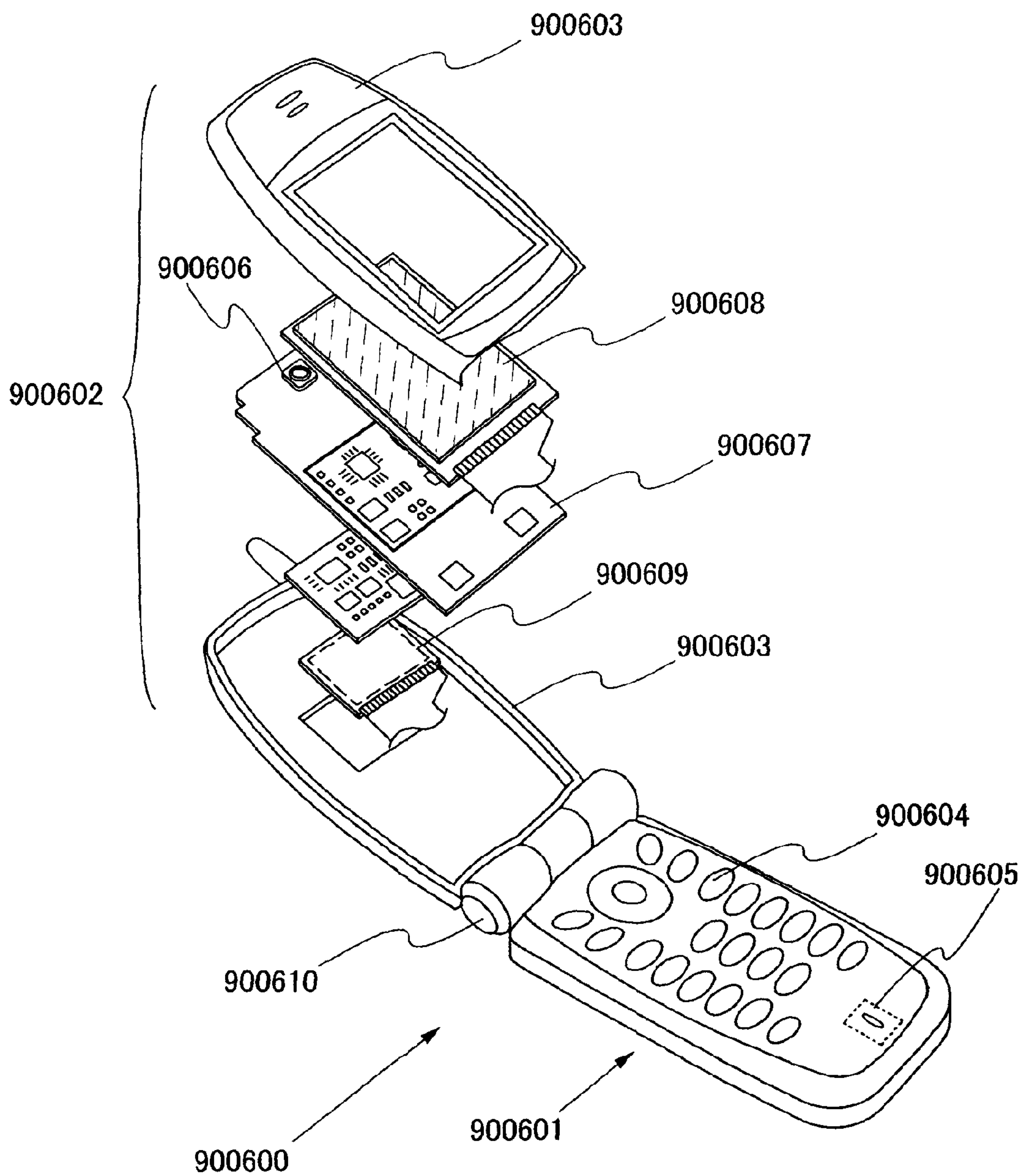

900603
900606
900608
900602
900607
900609
900603
900604
900605
900610
900600
900601

FIG. 81A

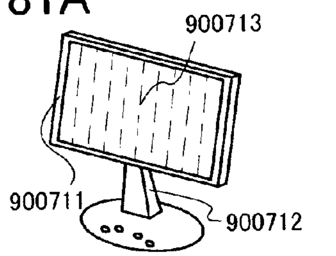


FIG. 81B

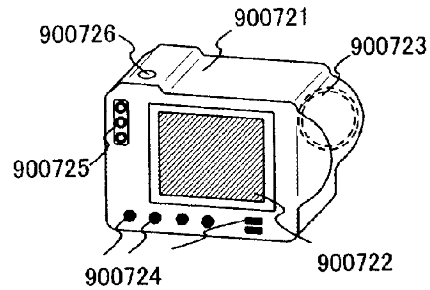


FIG. 81C

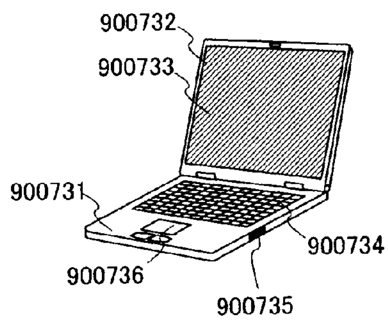


FIG. 81D

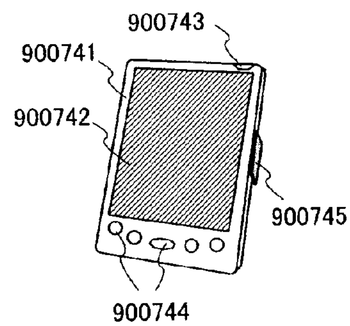


FIG. 81E

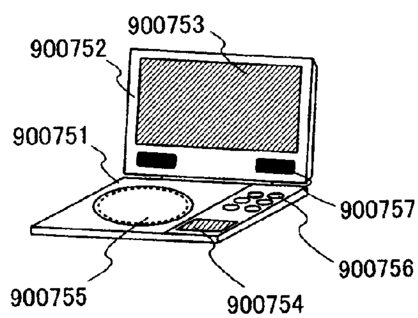


FIG. 81F

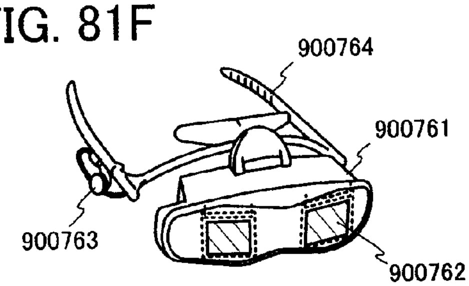


FIG. 81G

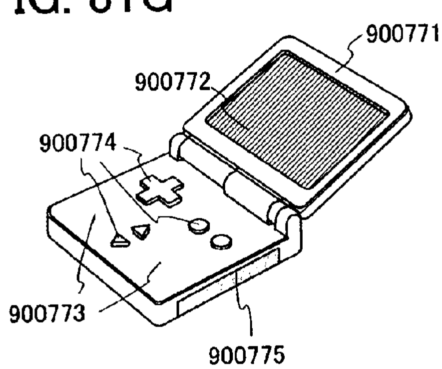


FIG. 81H

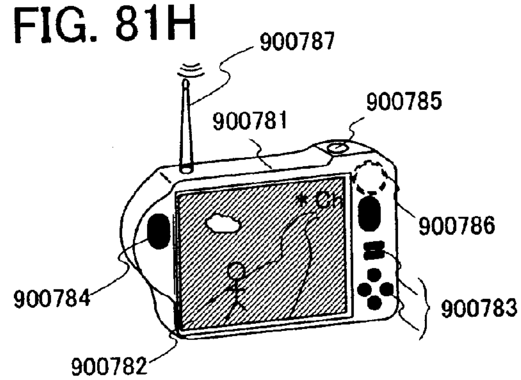


FIG. 82

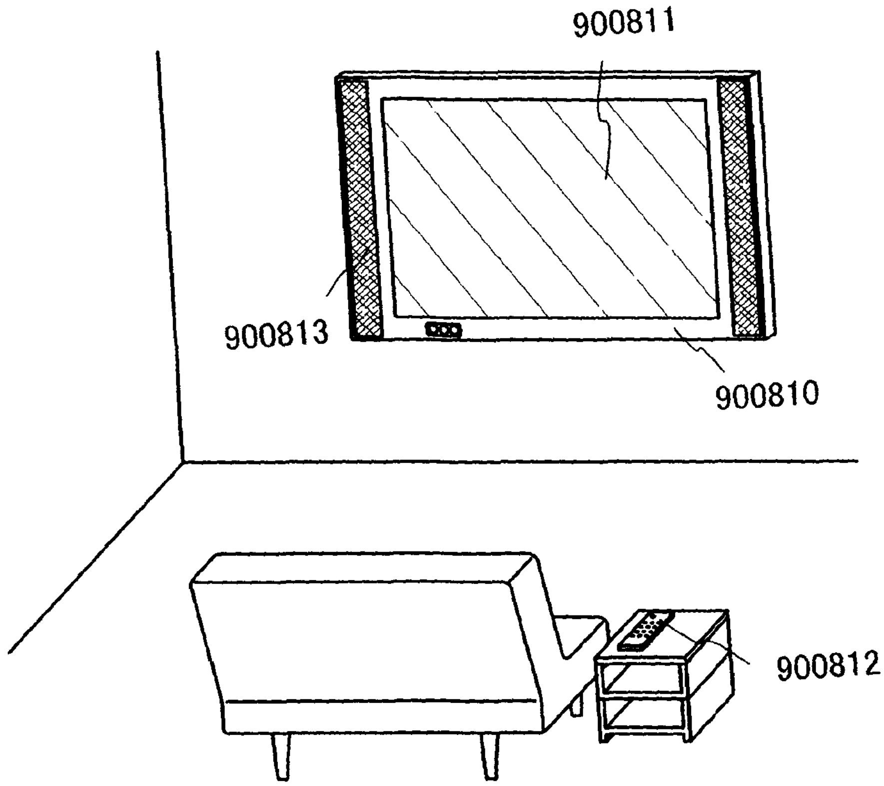


FIG. 83

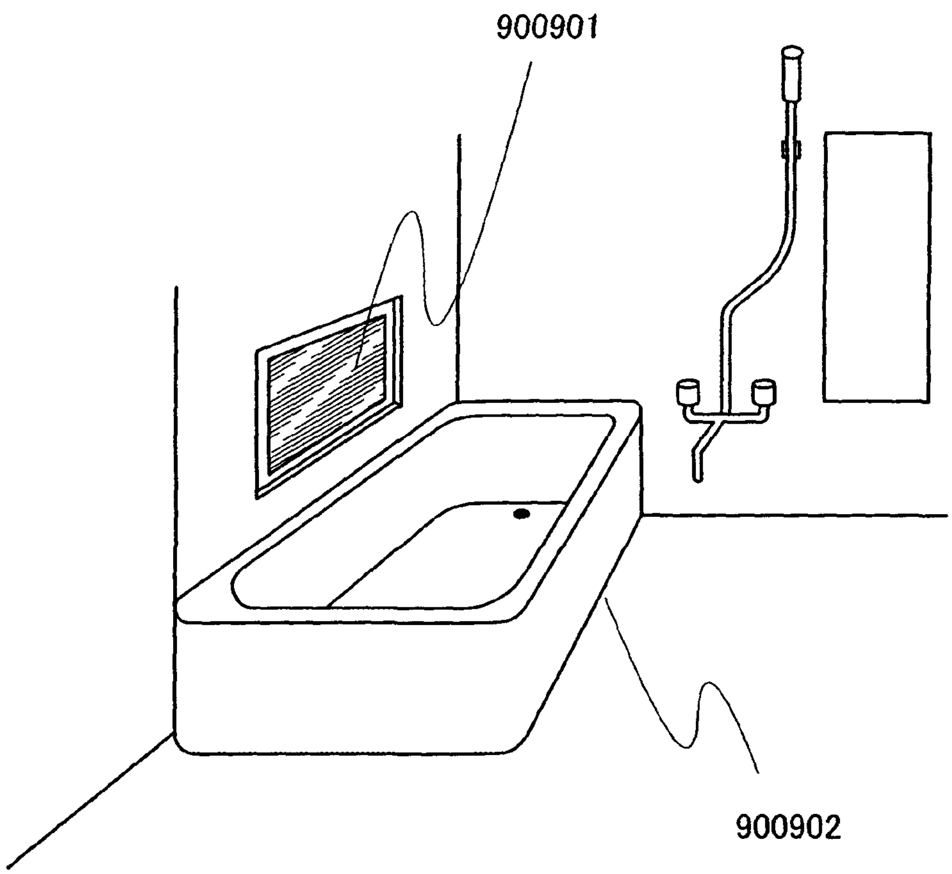


FIG. 84

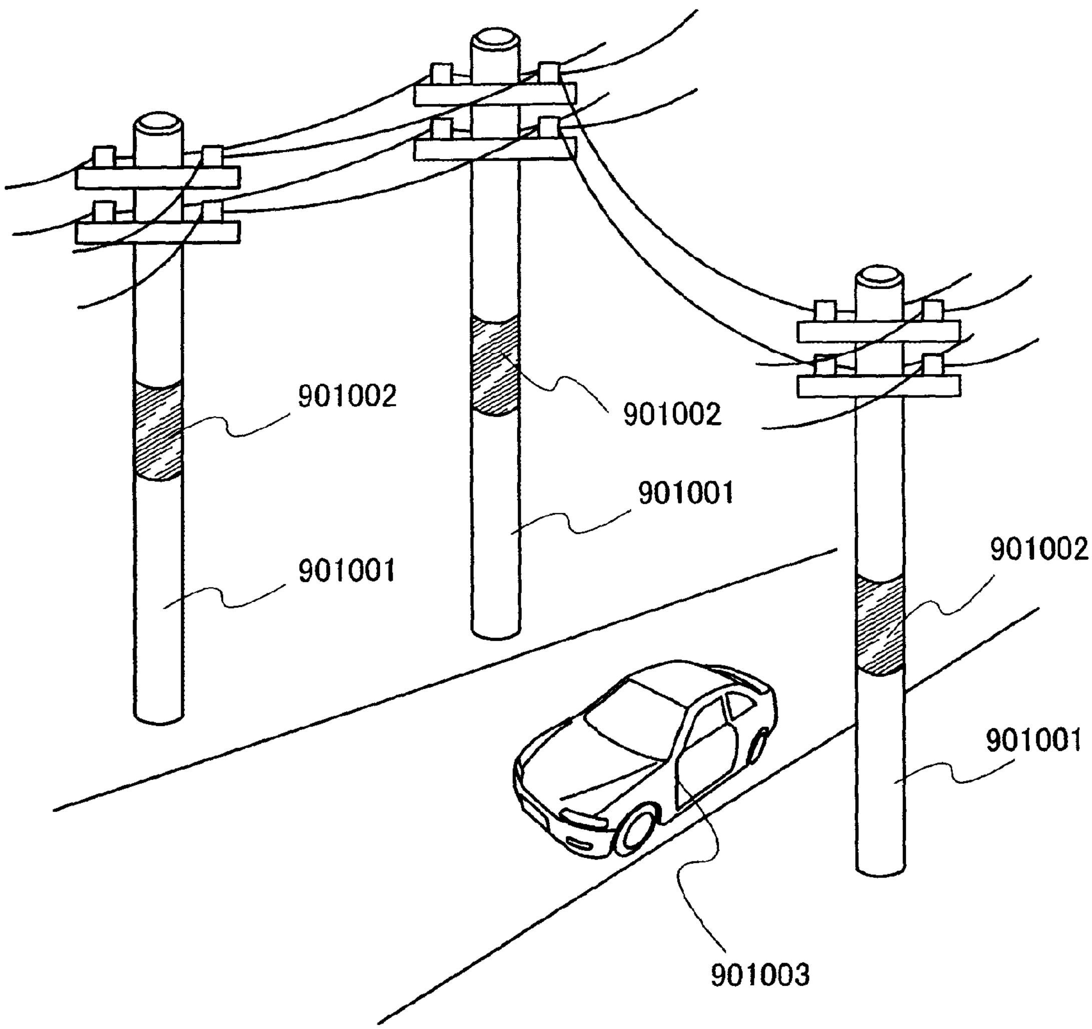


FIG. 85

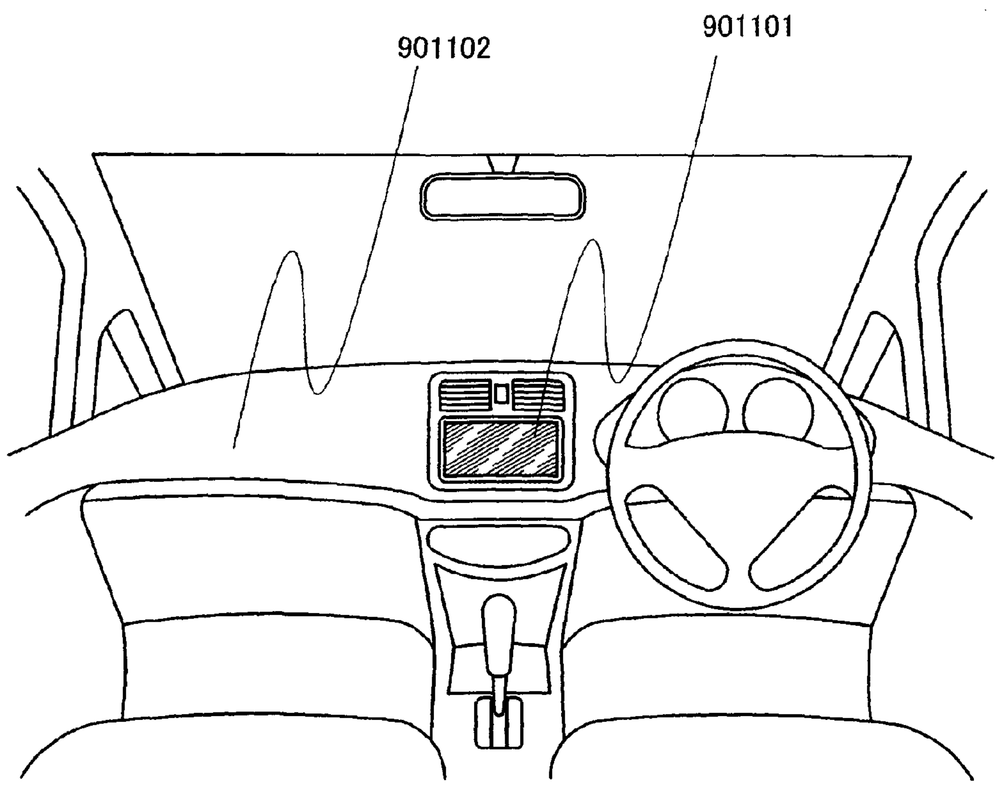


FIG. 86A

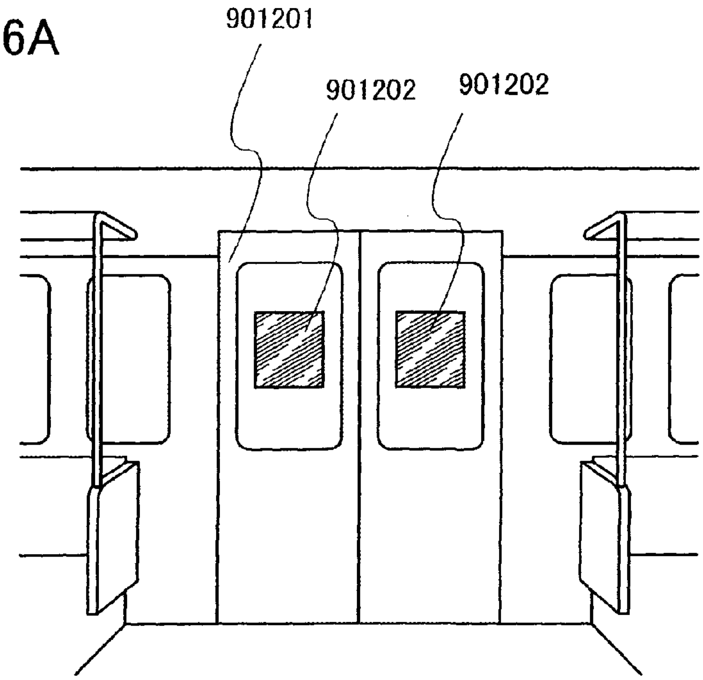


FIG. 86B

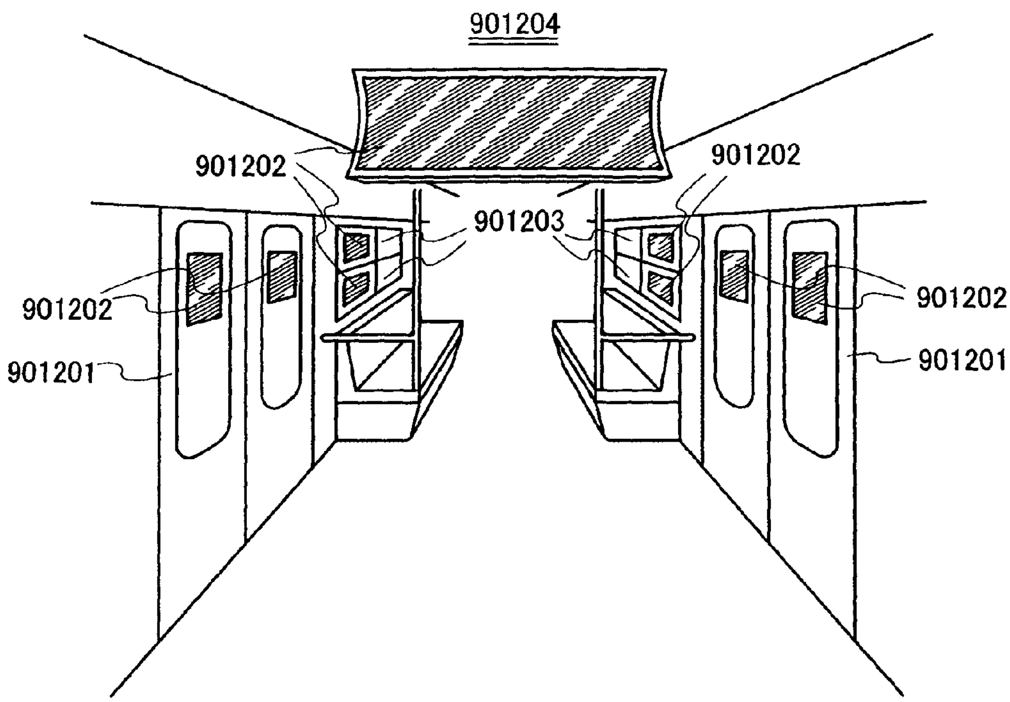


FIG. 87A

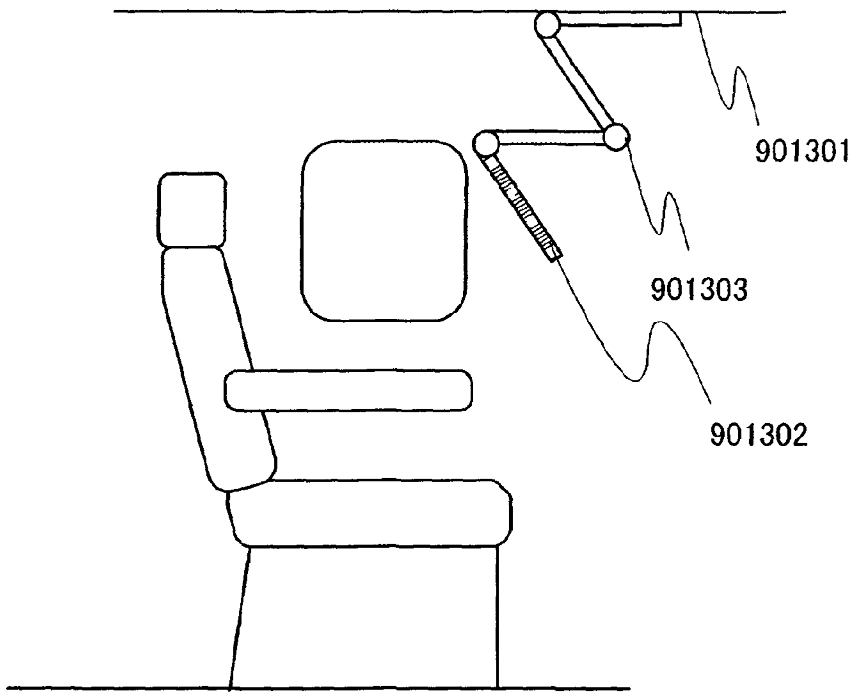
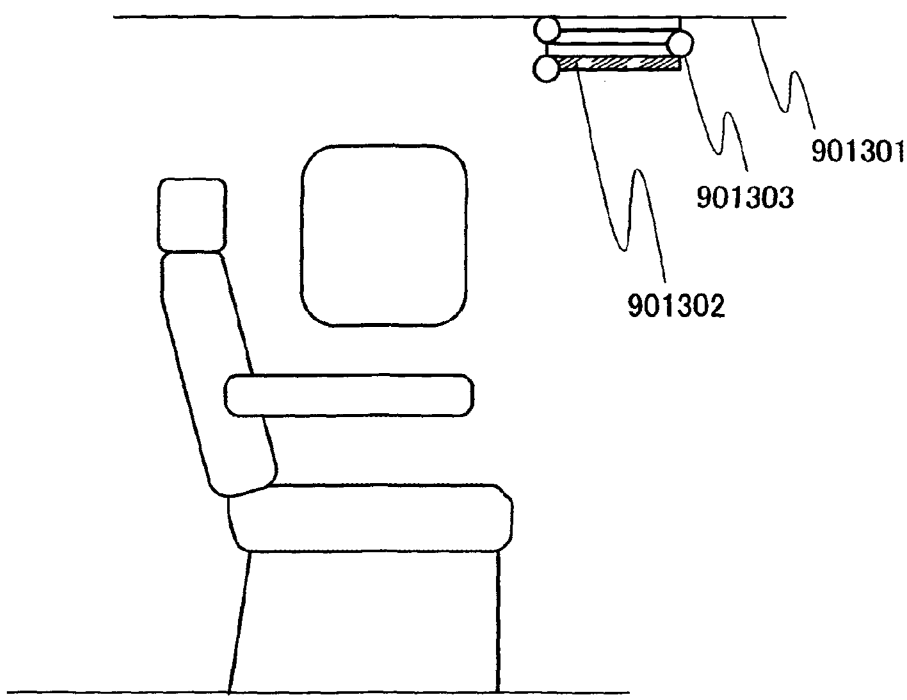


FIG. 87B



DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. application Ser. No. 11/972,159, filed Jan. 10, 2008, now allowed, which claims the benefit of a foreign priority application filed in Japan as Serial No. 2007-004106 on Jan. 12, 2007, both of which are incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an active matrix display device in which input of a video signal to a pixel can be controlled by a driver circuit.

2. Description of the Related Art

In an active matrix display device, a switching element and a display element are provided in each of hundreds of thousand to millions of pixels arranged in matrix. Since application of voltage or supply of current to the display element is held to some extent by the switching element after a video signal is input to the pixel, the active matrix display device can be flexible on enlargement and high definition of a panel and has become the mainstream of future display devices.

There are a scan line driver circuit and a signal line driver circuit as typical examples of a driver circuit included in the display device. A plurality of pixels in one line or a plurality of lines are selected at one time by a scan line driver circuit. In addition, input of video signals to the pixels included in the selected line is controlled by a signal line driver circuit.

These scan line driver circuit and signal line driver circuit need driving at high frequency. In particular, while pixels of respective lines are selected by the scan line driver circuit, the signal line driver circuit needs to input video signals to all the pixels in the lines. Thus, driving frequency of the signal line driver circuit is extremely higher than that of the scan line driver circuit. For example, in the case of a VGA active matrix display device, driving frequency of a signal line driver circuit generally needs to be approximately 25 MHz. Further, in recent years, the number of pixels in one line of an active matrix display device has been increased because an image with higher definition, higher resolution and more grayscales is displayed. Therefore, the signal line driver circuit needs driving at higher speed, and there has been a problem in that power consumption is high due to high driving frequency.

In view of the foregoing problem, Reference 1 (Japanese Patent No. 3338259) discloses a liquid crystal display device in which pieces of display data corresponding to adjacent two scan lines are compared with each other and transmission of the pieces of display data to the signal line driver circuit is not performed when the pieces of display data correspond to each other in order to suppress power consumption of a signal line driver circuit.

Further, Reference 2 (Japanese Patent No. 3593392) discloses a liquid crystal display device in which a wiring between a control IC and a signal line driver circuit is made shorter by providing the control IC so that output pins to the signal line driver circuit are close to the signal line driver circuit, so that power consumption due to wiring capacitance is suppressed.

SUMMARY OF THE INVENTION

It is naturally expected that lines where pieces of data correspond to each other exist discontinuously when an

image is actually displayed. However, only comparison of pieces of data corresponding to adjacent lines can be performed by using the technique disclosed in Reference 1. Therefore, even when pieces of data of input video signals correspond to each other in a plurality of lines, input of video signals to a signal line driver circuit cannot be omitted when there is even only one line corresponding to another data among the plurality of lines.

In addition, there is a natural possibility that a plurality of groups of a plurality of lines corresponding to the same data exist such that a group of a plurality of lines having the same data and a group of a plurality of lines having another data exist. In this case, since only comparison of pieces of data corresponding to adjacent lines can be performed by using the technique disclosed in Reference 1, input of video signals to a signal line driver circuit cannot be omitted.

Thus, there is a problem in that power consumption of a signal line driver circuit and power consumption of the entire display device cannot efficiently suppressed even when the technique disclosed in Reference 1 is used.

In addition, there is also a problem in that there is limitation on reduction in power consumption of the entire display device by just devising leading of wirings as disclosed in Reference 2.

In view of the foregoing problems, it is an object of the present invention to provide an active matrix display device in which power consumption of a signal line driver circuit can be suppressed, so that power consumption of the entire appliance can be suppressed.

In a display device of the present invention, a plurality of memory circuits which can write data of a video signal input to a pixel in one line period and can hold the data are provided in a driver circuit. The memory circuit includes a plurality of memory elements and holds data input to pixels for one line in the plurality of memory elements. Then, the data stored in each memory circuit is input to pixels in a corresponding line as a video signals. Since the display device of the present invention includes two or more memory circuits in the driver circuit, pieces of data of video signals corresponding to two or more line periods which appear discontinuously can be concurrently held in the memory circuits. Note that a line period corresponds to a period during which pixels of each line are selected by a scan line driver circuit and signals are input to the selected pixel.

The display device of the present invention includes a memory which can store data of video signals corresponding to a plurality of line periods or a plurality of frame periods, and a data comparison portion which reads data of video signals corresponding to respective line periods from the memory and compares the data with data of video signals corresponding to other line periods.

Then, the data comparison portion controls writing and holding of data in each memory circuit in accordance with the comparison result. Specifically, by comparing the pieces of data of the video signals corresponding to respective line periods, the data comparison portion extracts a plurality of line periods in which pieces of data correspond to each other. Then, after the data comparison portion writes the corresponding data to the memory circuits, the data comparison portion makes the memory circuits hold the data without being rewritten until the video signals having the data are input to the pixels in all the extracted line periods. Further, when input of the video signals in all the extracted line periods is completed, the data comparison portion can rewrite the data stored in the memory circuits into another data.

Note that as the display device of the present invention, an active matrix display device such as a liquid crystal display device, a light-emitting device provided with a light-emitting element typified by an organic light-emitting element (OLED) in each pixel, a DMD (digital micromirror device), a PDP (plasma display panel), or an FED (field emission display) is included in its category. In addition, a passive matrix display device is included in its category.

Various types of switches can be used as a switch shown in this document. An electrical switch, a mechanical switch, and the like are given as examples. That is, any element can be used as long as it can control a current flow, without limiting to a certain element. For example, a transistor (e.g., a bipolar transistor or a MOS transistor), a diode (e.g., a PN diode, a PIN diode, a Schottky diode, an MIM (metal insulator metal) diode, an MIS (metal insulator semiconductor) diode, or a diode-connected transistor), a thyristor, or the like can be used as a switch. Alternatively, a logic circuit combining such elements can be used as a switch.

In the case of using a transistor as a switch, polarity (a conductivity type) of the transistor is not particularly limited because it operates just as a switch. However, a transistor of polarity with smaller off-current is preferably used when off-current is to be suppressed. A transistor provided with an LDD region, a transistor with a multi-gate structure, and the like are given as examples of a transistor with smaller off-current. In addition, it is preferable that an N-channel transistor be used when a potential of a source terminal is closer to a potential of a low-potential-side power supply (e.g., V_{ss}, GND, or 0 V), while a P-channel transistor be used when the potential of the source terminal is closer to a potential of a high-potential-side power supply (e.g., V_{dd}). This is because the absolute value of gate-source voltage can be increased when the potential of the source terminal is closer to a potential of a low-potential-side power supply in an N-channel transistor and when the potential of the source terminal is closer to a potential of a high-potential-side power supply in a P-channel transistor. This is also because the transistor does not often perform a source follower operation, so that reduction in output voltage does not often occur.

Note that a CMOS switch using both N-channel and P-channel transistors may be used. By using a CMOS switch, the switch can easily operate as a switch because current can flow when the P-channel transistor or the N-channel transistor is turned on. For example, voltage can be appropriately output regardless of whether voltage of an input signal of the switch is high or low. In addition, since a voltage amplitude value of a signal for turning on or off the switch can be made small, power consumption can be reduced.

When a transistor is used as a switch, the switch includes an input terminal (one of a source terminal and a drain terminal), an output terminal (the other of the source terminal and the drain terminal), and a terminal for controlling electrical conduction (a gate terminal). On the other hand, when a diode is used as a switch, the switch does not have a terminal for controlling electrical conduction in some cases. Therefore, when a diode is used as a switch, the number of wirings for controlling terminals can be more reduced than the case of using a transistor as a switch.

In this document, when it is described that "A and B are connected", the case where A and B are electrically connected, the case where A and B are functionally connected, and the case where A and B are directly connected are included therein. Here, each of A and B corresponds to an object (e.g., a device, an element, a circuit, a wiring, an electrode, a terminal, a conductive film, or a layer). Accordingly, in structures disclosed in this document, another element may be interposed between elements having a connection relation shown in drawings and texts, without limiting to a predetermined connection relation, for example, the connection relation shown in the drawings and the texts.

For example, in the case where A and B are electrically connected, one or more elements which enable electrical connection of A and B (e.g., a switch, a transistor, a capacitor, an inductor, a resistor, and/or a diode) may be provided between A and B. In addition, in the case where A and B are functionally connected, one or more circuits which enable functional connection of A and B (e.g., a logic circuit such as an inverter, a NAND circuit, or a NOR circuit, a signal converter circuit such as a DA converter circuit, an AD converter circuit, or a gamma correction circuit, a potential level converter circuit such as a power supply circuit (e.g., a boosting circuit or a voltage lower control circuit) or a level shifter circuit for changing a potential level of a signal, a voltage source, a current source, a switching circuit, or an amplifier circuit such as a circuit which can increase signal amplitude, the amount of current, or the like (e.g., an operational amplifier, a differential amplifier circuit, a source follower circuit, or a buffer circuit), a signal generating circuit, a memory circuit, and/or a control circuit) may be provided between A and B. Alternatively, in the case where A and B are directly connected, A and B may be directly connected without interposing another element or another circuit therebetween.

When it is described that "A and B are directly connected", the case where A and B are directly connected (i.e., the case where A and B are connected without interposing another element or another circuit therebetween) and the case where A and B are electrically connected (i.e., the case where A and B are connected by interposing another element or another circuit therebetween) are included therein.

When it is described that "A and B are electrically connected", the case where A and B are electrically connected (i.e., the case where A and B are connected by interposing another element or another circuit therebetween), the case where A and B are functionally connected (i.e., the case where A and B are functionally connected by interposing another circuit therebetween), and the case where A and B are directly connected (i.e., the case where A and B are connected without interposing another element or another circuit therebetween) are included therein. That is, when it is described that "A and B are electrically connected", the description is the same as the case where it is explicitly only described that "A and B are connected".

A display element, a display device which is a device having a display element, a light-emitting element, and a light-emitting device which is a device having a light-emitting element can use various types and can include various elements. For example, as a display element, a display device, a light-emitting element, and a light-emitting device, whose a display medium, contrast, luminance, reflectivity, transitivity, or the like changes by an electromagnetic action, such as an EL element (e.g., an EL element including organic and inorganic materials, an organic EL element, or an inorganic EL element), an electron emitter, a liquid crystal element, electronic ink, an electrophoresis element, a grating light valve (GLV), a plasma display panel (PDP), a digital micromirror device (DMD), a piezoelectric ceramic display, or a carbon nanotube can be used. Note that display devices using an EL element include an EL display; display devices using an electron emitter include a field emission display (FED), an SED-type flat panel display (SED: Surface-conduction Electron-emitter Display), and the like; display devices using a liquid crystal element include a liquid crystal display (e.g., a transmissive liquid crystal display, a semi-transmissive liquid crystal display, a reflective liquid crystal display, a direct-view liquid crystal display, or a projection liquid crystal display); and display devices using electronic ink or an electrophoresis element include electronic paper.

By using a catalyst (e.g., nickel) in the case of forming microcrystalline silicon, crystallinity can be further improved and a transistor having excellent electric characteristics can be formed. At this time, crystallinity can be improved by performing heat treatment without using a laser. Accordingly, a gate driver circuit (e.g., a scan line driver circuit) and part of a source driver circuit (e.g., an analog switch) can be formed over the same substrate. In addition, in the case of not using a laser for crystallization, crystallinity unevenness of silicon can be suppressed. Therefore, an image having high quality can be displayed.

Note that polycrystalline silicon and microcrystalline silicon can be formed without using a catalyst (e.g., nickel).

A transistor can be formed by using a semiconductor substrate, an SOI substrate, or the like. Thus, a transistor with few variations in characteristics, sizes, shapes, or the like, with high current supply capacity, and with a small size can be formed. By using such a transistor, power consumption of a circuit can be reduced or a circuit can be highly integrated.

A transistor including a compound semiconductor or an oxide semiconductor such as ZnO, a-InGaZnO, SiGe, GaAs, IZO, ITO, or SnO, a thin film transistor obtained by thinning such a compound semiconductor or a oxide semiconductor, or the like can be used. Thus, manufacturing temperature can be lowered and for example, such a transistor can be formed at room temperature. Accordingly, the transistor can be formed directly on a substrate having low heat resistance such as a plastic substrate or a film substrate. Note that such a compound semiconductor or an oxide semiconductor can be used for not only a channel portion of the transistor but also other applications. For example, such a compound semiconductor or an oxide semiconductor can be used as a resistor, a pixel electrode, or a light-transmitting electrode. Further, since such an element can be formed at the same time as the transistor, cost can be reduced.

A transistor formed by using an inkjet method or a printing method, or the like can be used. Accordingly, a transistor can be formed at room temperature, can be formed at a low vacuum, or can be formed using a large substrate. In addition, since the transistor can be formed without using a mask (a reticle), a layout of the transistor can be easily changed. Further, since it is not necessary to use a resist, material cost is reduced and the number of steps can be reduced. Furthermore, since a film is formed only in a necessary portion, a material is not wasted compared with a manufacturing method in which etching is performed after the film is formed over the entire surface, so that cost can be reduced.

A transistor including an organic semiconductor or a carbon nanotube, or the like can be used. Accordingly, such a transistor can be formed using a substrate which can be bent. Therefore, a device using a transistor including an organic semiconductor or a carbon nanotube, or the like can resist a shock.

Further, transistors with various structures can be used. For example, a MOS transistor, a junction transistor, a bipolar transistor, or the like can be used as a transistor described in this document. By using a MOS transistor, the size of the transistor can be reduced. Thus, a large number of transistors can be mounted. By using a bipolar transistor, large current can flow. Thus, a circuit can be operated at high speed.

Note that a MOS transistor, a bipolar transistor, and the like may be formed over one substrate. Thus, reduction in power consumption, reduction in size, high speed operation, and the like can be realized.

Furthermore, various transistors can be used.

A transistor can be formed using various types of substrates. The type of a substrate where a transistor is formed is not limited to a certain type. For example, a single crystalline substrate, an SOI substrate, a glass substrate, a quartz substrate, a plastic substrate, a paper substrate, a cellophane substrate, a stone substrate, a wood substrate, a cloth substrate (including a natural fiber (e.g., silk, cotton, or hemp), a synthetic fiber (e.g., nylon, polyurethane, or polyester), a regenerated fiber (e.g., acetate, cupra, rayon, or regenerated polyester), or the like), a leather substrate, a rubber substrate, a stainless steel substrate, a substrate including a stainless steel foil, or the like can be used as a substrate where the transistor is formed. Alternatively, a skin (e.g., epidermis or corium) or hypodermal tissue of an animal such as a human being can be used as a substrate where the transistor is formed. In addition, the transistor may be formed using one substrate, and then, the transistor may be transferred to another substrate. A single crystalline substrate, an SOI substrate, a glass substrate, a quartz substrate, a plastic substrate, a paper substrate, a cellophane substrate, a stone substrate, a wood substrate, a cloth substrate (including a natural fiber (e.g., silk, cotton, or hemp), a synthetic fiber (e.g., nylon, polyurethane, or polyester), a regenerated fiber (e.g., acetate, cupra, rayon, or regenerated polyester), or the like), a leather substrate, a rubber substrate, a stainless steel substrate, a substrate including a stainless steel foil, or the like can be used as a substrate to which the transistor is transferred. Alternatively, a skin (e.g., epidermis or corium) or hypodermal tissue of an animal such as a human being can be used as a substrate to which the transistor is transferred. Further alternatively, the transistor may be formed using one substrate and the substrate may be thinned by polishing. A single crystalline substrate, an SOI substrate, a glass substrate, a quartz substrate, a plastic substrate, a paper substrate, a cellophane substrate, a stone substrate, a wood substrate, a cloth substrate (including a natural fiber (e.g., silk, cotton, or hemp), a synthetic fiber (e.g., nylon, polyurethane, or polyester), a regenerated fiber (e.g., acetate, cupra, rayon, or regenerated polyester), or the like), a leather substrate, a rubber substrate, a stainless steel substrate, a substrate including a stainless steel foil, or the like can be used as a substrate to be polished. Alternatively, a skin (e.g., epidermis or corium) or hypodermal tissue of an animal such as a human being can be used as a substrate to be polished. By using such a substrate, a transistor with excellent properties or a transistor with low power consumption can be formed, a device with high durability, high heat resistance can be provided, or reduction in weight or thickness can be achieved.

A structure of a transistor can be various modes without limiting to a certain structure. For example, a multi-gate structure having two or more gate electrodes may be used. When the multi-gate structure is used, a structure where a plurality of transistors are connected in series is provided because a structure where channel regions are connected in series is provided. By using the multi-gate structure, off-current can be reduced or the withstand voltage of the transistor can be increased to improve reliability. Alternatively, by using the multi-gate structure, drain-source current does not fluctuate very much even if drain-source voltage fluctuates when the transistor operates in a saturation region, so that a flat slope of voltage-current characteristics can be obtained. By utilizing the flat slope of the voltage-current characteristics, an ideal current source circuit or an active load having a high resistance value can be realized. Accordingly, a differential circuit or a current mirror circuit having excellent properties can be realized. In addition, a structure where gate electrodes are formed above and below a channel may be used. By using the structure where gate electrodes are formed above and below the channel, a channel region is enlarged, so that the amount of current flowing therethrough can be increased or a depletion layer can be easily formed to decrease an S value. When the gate electrodes are formed above and below the channel, a structure where a plurality of transistors are connected in parallel is provided.

Further, a structure where a gate electrode is formed above a channel formation region, a structure where a gate electrode is formed below a channel formation region, a staggered structure, an inversely staggered structure, a structure where a channel formation region is divided into a plurality of regions, or a structure where channel formation regions are connected in parallel or in series can be used. In addition, a source electrode or a drain electrode may overlap with a channel formation region (or part of it). By using the structure where the source electrode or the drain electrode may overlap with the channel formation region (or part of it), the case can be prevented in which electric charges are accumulated in part of the channel formation region, which would result in an unstable operation. Further, an LDD region may be provided. By providing the LDD region, off-current can be reduced or the withstand voltage of the transistor can be increased to improve reliability. Alternatively, by providing the LDD region, drain-source current does not fluctuate very much even if drain-source voltage fluctuates when the transistor operates in the saturation region, so that a flat slope of voltage-current characteristics can be obtained.

Various types of transistors can be used for a transistor in this document and the transistor can be formed using various types of substrates. Accordingly, all of circuits which are necessary to realize a predetermined function may be formed using the same substrate. For example, all of the circuits which are necessary to realize the predetermined function may be formed using a glass substrate, a plastic substrate, a single crystalline substrate, an SOI substrate, or any other substrate. When all of the circuits which are necessary to realize the predetermined function are formed using the same substrate, cost can be reduced by reduction in the number of component parts or reliability can be improved by reduction in the number of connections to circuit components. Alternatively, part of the circuits which are necessary to realize the predetermined function may be formed using one substrate and another part of the circuits which are necessary to realize the predetermined function may be formed using another substrate. That is, not all of the circuits which are necessary to realize the predetermined function are required to be formed using the same substrate. For example, part of the circuits which are necessary to realize the predetermined function may be formed with transistors using a glass substrate and another part of the circuits which are necessary to realize the predetermined function may be formed using a single crystalline substrate, so that an IC chip formed by a transistor using the single crystalline substrate may be connected to the glass substrate by COG (chip on glass) and the IC chip may be provided over the glass substrate. Alternatively, the IC chip may be connected to the glass substrate by TAB (tape automated bonding) or a printed wiring board. When part of the circuits are formed using the same substrate in this manner, cost can be reduced by reduction in the number of component parts or reliability can be improved by reduction in the number of connections to circuit components. In addition, for example, by forming a portion with high driving voltage or a portion with high driving frequency, which consumes large power, using a single crystalline substrate and using an IC chip formed by the circuit instead of forming such a portion using the same substrate, increase in power consumption can be prevented.

Note that one pixel corresponds to one element whose brightness can be controlled in this document. Therefore, for example, one pixel corresponds to one color element and brightness is expressed with the one color element. Accordingly, in the case of a color display device having color elements of R (red), G (green), and B (blue), a minimum unit of an image is formed of three pixels of an R pixel, a G pixel, and a B pixel. Note that the color elements are not limited to three colors, and color elements of more than three colors may be used or a color other than RGB may be used. For example, RGBW (W corresponds to white) may be used by adding white. In addition, one or more colors of yellow, cyan, magenta emerald green, vermilion, and the like may be added to RGB. Further, a color similar to at least one of R, G, and B may be added to RGB. For example, R, G, B1, and B2 may be used. Although both B1 and B2 are blue, they have slightly different frequency. Similarly, R1, R2, G, and B may be used. By using such color elements, display which is closer to the real object can be performed or power consumption can be reduced. Alternatively, as another example, in the case of controlling brightness of one color element by using a plurality of regions, one region may correspond to one pixel. Therefore, for example, in the case of performing area ratio gray scale display or the case of including a subpixel, a plurality of regions which control brightness are provided in each color element and gray scales are expressed with the whole regions. In this case, one region which controls brightness may correspond to one pixel. Thus, in that case, one color element includes a plurality of pixels. Alternatively, even when the plurality of regions which control brightness are provided in one color element, these regions may be collected as one pixel. Thus, in that case, one color element includes one pixel. In that case, one color element includes one pixel. In the case where brightness is controlled in a plurality of regions in each color element, regions which contribute to display have different area dimensions depending on pixels in some cases. In addition, in the plurality of regions which control brightness in each color element, signals supplied to each of the plurality of regions may be slightly varied to widen a viewing angle. That is, potentials of pixel electrodes included in the plurality of regions provided in each color element may be different from each other. Accordingly, voltage applied to liquid crystal molecules are varied depending on the pixel electrodes. Therefore, the viewing angle can be widened.

When it is described that "one pixel (for three colors)", it corresponds to the case where three pixels of R, G, and B are considered as one pixel. Meanwhile, when it is described that "one pixel (for one color)", it corresponds to the case where the plurality of regions are provided in each color element and collectively considered as one pixel.

In this document, pixels are provided (arranged) in matrix in some cases. Here, description that pixels are provided (arranged) in matrix includes the case where the pixels are arranged in a straight line and the case where the pixels are arranged in a jagged line, in a longitudinal direction or a lateral direction. Thus, for example, in the case of performing full color display with three color elements (e.g., RGB), the following cases are included therein: the case where the pixels are arranged in stripes and the case where dots of the three color elements are arranged in a delta pattern. In addition, the case is also included therein in which dots of the three color elements are provided in Bayer arrangement. Note that the color elements are not limited to three colors, and color elements of more than three colors may be used. RGBW (W corresponds to white), RGB plus one or more of yellow, cyan, magenta, and the like, or the like is given as an example. Further, the sizes of display regions may be different between respective dots of color elements. Thus, power consumption can be reduced or the life of a display element can be prolonged.

In this document, an active matrix method in which an active element is included in a pixel or a passive matrix method in which an active element is not included in a pixel can be used.

In an active matrix method, as an active element (a non-linear element), not only a transistor but also various active elements (non-linear elements) can be used. For example, an MIM (metal insulator metal), a TFD (thin film diode), or the like can also be used. Since such an element has few number of manufacturing steps, manufacturing cost can be reduced or yield can be improved. Further, since the size of the element is small, the aperture ratio can be improved, so that power consumption can be reduced or high luminance can be achieved.

As a method other than an active matrix method, a passive matrix method in which an active element (a non-linear element) is not used can also be used. Since an active element (a non-linear element) is not used, manufacturing steps is few, so that manufacturing cost can be reduced or the yield can be improved. Further, since an active element (a non-linear element) is not used, the aperture ratio can be improved, so that power consumption can be reduced or high luminance can be achieved.

A transistor is an element having at least three terminals of a gate, a drain, and a source. The transistor has a channel formation region between a drain region and a source region, and current can flow through the drain region, the channel formation region, and the source region. Here, since the source and the drain of the transistor may change depending on the structure, the operating condition, and the like of the transistor, it is difficult to define which is a source or a drain. Therefore, in this document, a region functioning as a source and a drain may not be called the source or the drain. In such a case, one of the source and the drain may be referred to as a first terminal and the other thereof may be referred to as a second terminal, for example. Alternatively, one of the source and the drain may be referred to as a first electrode and the other thereof may be referred to as a second electrode. Further alternatively, one of the source and the drain may be referred to as a source region and the other thereof may be called a drain region.

A transistor may be an element having at least three terminals of a base, an emitter, and a collector. In this case also, one of the emitter and the collector may be similarly called a first terminal and the other terminal may be called a second terminal.

A gate corresponds to all or part of a gate electrode and a gate wiring (also referred to as a gate line, a gate signal line, a scan line, a scan signal line, or the like). A gate electrode corresponds to a conductive film which overlaps with a semiconductor which forms a channel formation region with a gate insulating film interposed therebetween. Note that part of the gate electrode overlaps with an LDD (lightly doped drain) region, the source region, or the drain region with the gate insulating film interposed therebetween in some cases. A gate wiring corresponds to a wiring for connecting a gate electrode of each transistor to each other, a wiring for connecting a gate electrode of each pixel to each other, or a wiring for connecting a gate electrode to another wiring.

However, there is a portion (a region, a conductive film, a wiring, or the like) which functions as both a gate electrode and a gate wiring. Such a portion (a region, a conductive film, a wiring, or the like) may be called either a gate electrode or a gate wiring. That is, there is a region where a gate electrode and a gate wiring cannot be clearly distinguished from each other. For example, in the case where a channel formation region overlaps with part of an extended gate wiring, the overlapped portion (region, conductive film, wiring, or the like) functions as both a gate wiring and a gate electrode. Accordingly, such a portion (a region, a conductive film, a wiring, or the like) may be called either a gate electrode or a gate wiring.

A portion (a region, a conductive film, a wiring, or the like) which is formed using the same material as a gate electrode, forms the same island as the gate electrode, and is connected to the gate electrode may also be called a gate electrode. Similarly, a portion (a region, a conductive film, a wiring, or the like) which is formed using the same material as a gate wiring, forms the same island as the gate wiring, and is connected to the gate wiring may also be called a gate wiring. In a strict detect, such a portion (a region, a conductive film, a wiring, or the like) does not overlap with a channel formation region or does not have a function of connecting the gate electrode to another gate electrode in some cases. However, there is a portion (a region, a conductive film, a wiring, or the like) which is formed using the same material as a gate electrode or a gate wiring, forms the same island as the gate electrode or the gate wiring, and is connected to the gate electrode or the gate wiring. Thus, such a portion (a region, a conductive film, a wiring, or the like) may also be called either a gate electrode or a gate wiring.

In a multi-gate transistor, for example, a gate electrode is often connected to another gate electrode by using a conductive film which is formed using the same material as the gate electrode. Since such a portion (a region, a conductive film, a wiring, or the like) is a portion (a region, a conductive film, a wiring, or the like) for connecting the gate electrode to another gate electrode, it may be called a gate wiring, and it may also be called a gate electrode because a multi-gate transistor can be considered as one transistor. That is, a portion (a region, a conductive film, a wiring, or the like) which is formed using the same material as a gate electrode or a gate wiring, forms the same island as the gate electrode or the gate wiring, and is connected to the gate electrode or the gate wiring may be called either a gate electrode or a gate wiring. In addition, for example, part of a conductive film which connects the gate electrode and the gate wiring and is formed using a material which is different from that of the gate electrode or the gate wiring may also be called either a gate electrode or a gate wiring.

A gate terminal corresponds to part of a portion (a region, a conductive film, a wiring, or the like) of a gate electrode or a portion (a region, a conductive film, a wiring, or the like) which is electrically connected to the gate electrode.

When a wiring is called a gate wiring, a gate line, a gate signal line, a scan line, a scan signal line, there is the case in which a gate of a transistor is not connected to a wiring. In this case, the gate wiring, the gate line, the gate signal line, the scan line, or the scan signal line corresponds to a wiring formed in the same layer as the gate of the transistor, a wiring formed using the same material of the gate of the transistor, or a wiring formed at the same time as the gate of the transistor in some cases. As examples, a wiring for storage capacitance, a power supply line, a reference potential supply line, and the like can be given.

A source corresponds to all or part of a source region, a source electrode, and a source wiring (also referred to as a source line, a source signal line, a data line, a data signal line, or the like). A source region corresponds to a semiconductor region including a large amount of p-type impurities (e.g., boron or gallium) or n-type impurities (e.g., phosphorus or arsenic). Therefore, a region including a small amount of p-type impurities or n-type impurities, namely, an LDD (lightly doped drain) region is not included in the source region. A source electrode is part of a conductive layer formed using a material different from that of a source region, and electrically connected to the source region. However, there is the case where a source electrode and a source region are collectively called a source electrode. A source wiring is a wiring for connecting a source electrode of each transistor to each other, a wiring for connecting a source electrode of each pixel to each other, or a wiring for connecting a source electrode to another wiring.

However, there is a portion (a region, a conductive film, a wiring, or the like) functioning as both a source electrode and a source wiring. Such a portion (a region, a conductive film, a wiring, or the like) may be called either a source electrode or a source wiring. That is, there is a region where a source electrode and a source wiring cannot be clearly distinguished from each other. For example, in the case where a source region overlaps with part of an extended source wiring, the overlapped portion (region, conductive film, wiring, or the like) functions as both a source wiring and a source electrode. Accordingly, such a portion (a region, a conductive film, a wiring, or the like) may be called either a source electrode or a source wiring.

A portion (a region, a conductive film, a wiring, or the like) which is formed using the same material as a source electrode, forms the same island as the source electrode, and is connected to the source electrode, or a portion (a region, a conductive film, a wiring, or the like) which connects a source electrode and another source electrode may also be called a source electrode. Further, a portion which overlaps with a source region may be called a source electrode. Similarly, a portion (a region, a conductive film, a wiring, or the like) which is formed using the same material as a source wiring, forms the same island as the source wiring, and is connected to the source wiring may also be called a source wiring. In a strict detect, such a portion (a region, a conductive film, a wiring, or the like) does not have a function of connecting the source electrode to another source electrode in some cases. However, there is a portion (a region, a conductive film, a wiring, or the like) which is formed using the same material as a source electrode or a source wiring, forms the same island as the source electrode or the source wiring, and is connected to the source electrode or the source wiring. Thus, such a portion (a region, a conductive film, a wiring, or the like) may also be called either a source electrode or a source wiring.

For example, part of a conductive film which connects a source electrode and a source wiring and is formed using a material which is different from that of the source electrode or the source wiring may be called either a source electrode or a source wiring.

A source terminal corresponds to a source region, a source electrode, or a portion (a region, a conductive film, a wiring, or the like) which is electrically connected to the source electrode.

When a wiring is called a source wiring, a source line, a source signal line, a data line, a data signal line, there is the case in which a source (a drain) of a transistor is not connected to a wiring. In this case, the source wiring, the source line, the source signal line, the data line, or the data signal line corresponds to a wiring formed in the same layer as the source (the drain) of the transistor, a wiring formed using the same material of the source (the drain) of the transistor, or a wiring formed at the same time as the source (the drain) of the transistor in some cases. As examples, a wiring for storage capacitance, a power supply line, a reference potential supply line, and the like can be given.

The same can be said for a drain.

A semiconductor device corresponds to a device having a circuit including a semiconductor element (e.g., a transistor, a diode, or thyristor). The semiconductor device may also include all devices that can function by utilizing semiconductor characteristics. In addition, the semiconductor device corresponds to a device having a semiconductor material.

A display element corresponds to an optical modulation element, a liquid crystal element, a light-emitting element, an EL element (an organic EL element, an inorganic EL element, or an EL element including organic and inorganic materials), an electron emitter, an electrophoresis element, a discharging element, a light-reflective element, a light diffraction element, a digital micro device (DMD), or the like. Note that the present invention is not limited to this.

A display device corresponds to a device having a display element. The display device may include a plurality of pixels each having a display element. Note that that the display device may also include a peripheral driver circuit for driving the plurality of pixels. The peripheral driver circuit for driving the plurality of pixels may be formed over the same substrate as the plurality of pixels. The display device may also include a peripheral driver circuit provided over a substrate by wire bonding or bump bonding, namely, an IC chip connected by chip on glass (COG) or an IC chip connected by TAB or the like. Further, the display device may also include a flexible printed circuit (an FPC) to which an IC chip, a resistor, a capacitor, an inductor, a transistor, or the like is attached. Note also that the display device includes a printed wiring board (a PWB) which is connected through a flexible printed circuit (an FPC) and to which an IC chip, a resistor, a capacitor, an inductor, a transistor, or the like is attached. The display device may also include an optical sheet such as a polarizing plate or a retardation plate. The display device may also include a lighting device, a housing, an audio input and output device, a light sensor, or the like. Here, a lighting device such as a backlight unit may include a light guide plate, a prism sheet, a diffusion sheet, a reflective sheet, a light source (e.g., an LED or a cold cathode fluorescent lamp), a cooling device (e.g., a water cooling device or an air cooling device), or the like.

A lighting device corresponds to a device having a backlight unit, a light guide plate, a prism sheet, a diffusion sheet, a reflective sheet, or a light source (e.g., an LED, a cold cathode fluorescent lamp, or a hot cathode fluorescent lamp), a cooling device, or the like.

A light-emitting device corresponds to a device having a light-emitting element and the like. In the case of including a light-emitting element as a display element, the light-emitting device is one of specific examples of a display device.

A reflective device corresponds to a device having a light-reflective element, a light diffraction element, light-reflective electrode, or the like.

A liquid crystal display device corresponds to a display device including a liquid crystal element. Liquid crystal display devices include a direct-view liquid crystal display, a projection liquid crystal display, a transmissive liquid crystal display, a reflective liquid crystal display, a semi-transmissive liquid crystal display, and the like.

A driving device corresponds to a device having a semiconductor element, an electric circuit, or an electronic circuit. For example, a transistor which controls input of a signal from a source signal line to a pixel (also referred to as a selection transistor, a switching transistor, or the like), a transistor which supplies voltage or current to a pixel electrode, a transistor which supplies voltage or current to a light-emitting element, and the like are examples of the driving device. A circuit which supplies a signal to a gate signal line (also referred to as a gate driver, a gate line driver circuit, or the like), a circuit which supplies a signal to a source signal line (also referred to as a source driver, a source line driver circuit, or the like) are also examples of the driving device.

A display device, a semiconductor device, a lighting device, a cooling device, a light-emitting device, a reflective device, a driving device, and the like overlap with each other in some cases. For example, a display device includes a semiconductor device and a light-emitting device in some cases. Alternatively, a semiconductor device includes a display device and a driving device in some cases.

In this document, when it is described that "B is formed on A" or "B is formed over A", it does not necessarily mean that B is formed in direct contact with A. The description includes the case where A and B are not in direct contact with each other, i.e., the case where another object is interposed between A and B. Here, each of A and B corresponds to an object (e.g., a device, an element, a circuit, a wiring, an electrode, a terminal, a conductive film, or a layer).

Accordingly, for example, when it is described that a layer B is formed on (or over) a layer A, it includes both the case where the layer B is formed in direct contact with the layer A, and the case where another layer (e.g., a layer C or a layer D) is formed in direct contact with the layer A and the layer B is formed in direct contact with the layer C or D. Note that another layer (e.g., a layer C or a layer D) may be a single layer or a plurality of layers.

Similarly, when it is described that B is formed above A, it does not necessarily mean that B is formed in direct contact with A, and another object may be interposed therebetween. Thus, for example, when it is described that a layer B is formed above a layer A, it includes both the case where the layer B is formed in direct contact with the layer A, and the case where another layer (e.g., a layer C or a layer D) is formed in direct contact with the layer A and the layer B is formed in direct contact with the layer C or D. Note that another layer (e.g., a layer C or a layer D) may be a single layer or a plurality of layers.

Note that when it is described that B is formed in direct contact with A, it includes not the case where another object is interposed between A and B but the case where B is formed in direct contact with A.

Note that the same can be said when it is described that B is formed below or under A.

In this document, when an object is explicitly described in a singular form, the object is preferably singular. Note that the present invention is not limited to this, and the object can be plural. Similarly, when an object is explicitly described in a plural form, the object is preferably plural. Note that the present invention is not limited to this, and the object can be singular.

Since the display device of the present invention includes a plurality of memory circuits in a driver circuit, pieces of data of video signals corresponding to a plurality of line periods can be held concurrently. Therefore, even when there are a plurality of line periods each having the same data and there is a line period corresponding to another data among the plurality of line periods, the corresponding data and another data can be held in different memory circuits. Thus, in the memory circuit in which the corresponded data is held, it is not necessary to rewrite data until the plurality of line periods are completed. That is, input of video signals to a signal line driver circuit, sampling of the video signals in the signal line driver circuit, and writing of data of the sampled video signals to a memory circuit can be performed at one time during the plurality of line periods.

Therefore, even when a plurality of line periods where pieces of data correspond to each other exist discontinuously, power consumption of the signal line driver circuit can be efficiently suppressed. Further, power consumption which is necessary for input of video signals to the signal line driver circuit can be suppressed, so that power consumption of the entire display device can be suppressed.

In addition, since the display device of the present invention includes the plurality of memory circuits, even when a plurality of groups each having a plurality of line periods where pieces of data correspond to each other exist, pieces of data corresponding to respective groups can be held in different memory circuits. Thus, it is not necessary to rewrite data in the memory circuit where the data is held until all the line periods in the group corresponding to the data are completed. That is, input of video signals to the signal line driver circuit, sampling of the video signals in the signal line driver circuit, and writing of data of the sampled video signals to the memory circuit can be performed at one time during all the line periods in one group.

Therefore, even when a plurality of groups each having a plurality of line periods where pieces of data correspond to each other exist, power consumption of the signal line driver circuit can be efficiently suppressed. Further, power consumption which is necessary for input of video signals to the signal line driver circuit can be suppressed, so that power consumption of the entire display device can be suppressed.

Further, in the display device of the present invention, by storing data of video signals corresponding to a plurality of line periods or a plurality of frame periods in a memory, a data comparison portion can compare data of a video signal corresponding to one line period with data of a video signal corresponding to a plurality of line periods other than one line period. Thus, comparison with not only data corresponding to adjacent line periods but also data corresponding to more line periods can be performed, so that power consumption of the signal line driver circuit can be efficiently suppressed.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIG. **1** is a block diagram illustrating a structure of a display device of the present invention;

FIGS. **2**A and **2**B each illustrate an operation of a signal line driver circuit in a display device of the present invention;

FIGS. **3**A and **3**B each illustrate an operation of a signal line driver circuit in a display device of the present invention;

FIGS. **4**A and **4**B each illustrate an operation of a signal line driver circuit in a display device of the present invention;

FIG. **5** is a timing chart illustrating a driving method of a display device of the present invention;

FIG. **6** is a block diagram illustrating a structure of a display device of the present invention;

FIG. **7** is a block diagram illustrating a structure of a data comparison portion;

FIG. **8** is a block diagram illustrating a structure of a data comparison portion;

FIG. **9** is a block diagram illustrating a structure of a display device of the present invention;

FIG. **10** is a block diagram illustrating a structure of a data comparison portion;

FIG. **11** is a block diagram illustrating a structure of a display device of the present invention;

FIG. **12** is a block diagram illustrating a structure of a display device of the present invention;

FIGS. **13**A and **13**B are timing charts each illustrating timing at which a video signal is input to a pixel portion;

FIG. **14** is a circuit diagram of a signal line driver circuit in a display device of the present invention;

FIG. **15** is a circuit diagram of a signal line driver circuit in a display device of the present invention;

FIGS. **16**A and **16**B are circuit diagrams each illustrating a structure of a pixel portion of a light-emitting device;

FIG. **17** is a circuit diagram illustrating a structure of a pixel portion of a liquid crystal display device;

FIG. **18**A is a top plan view of a display device of the present invention, and FIG. **18**B is a cross-sectional view of the display device of the present invention;

FIGS. **19**A to **19**C each illustrate an electronic device using a display device of the present invention;

FIG. **20** is a circuit diagram of a memory element;

FIG. **21** is a block diagram illustrating a structure of a data comparison portion;

FIG. **22** illustrates an example of a cross-sectional view of a display device in accordance with the present invention;

FIGS. **23**A and **23**B each illustrate an example of a cross-sectional view of a display device in accordance with the present invention;

FIGS. **24**A and **24**B each illustrate an example of a cross-sectional view of a display device in accordance with the present invention;

FIG. **25** illustrates an example of a pixel layout of a display device in accordance with the present invention;

FIGS. **26**A and **26**B each illustrate an example of a pixel layout of a display device in accordance with the present invention;

FIGS. **27**A and **27**B each illustrate an example of a pixel layout of a display device in accordance with the present invention;

FIG. **28** illustrates an example of a cross-sectional view of a display device in accordance with the present invention;

FIGS. **29**A to **29**D each illustrate an example of a peripheral component of a display device in accordance with the present invention;

FIG. **30** illustrates an example of a peripheral component of a display device in accordance with the present invention;

FIGS. **31**A to **31**C each illustrate an example of a circuit structure of a panel of a display device in accordance with the present invention;

FIGS. **32**A and **32**B each illustrate an example of a cross-sectional view of a display device in accordance with the present invention;

FIGS. **33**A to **33**C each illustrate an example of a driving method of a display device in accordance with the present invention;

FIGS. **34**A and **34**B each illustrate an example of a circuit structure of a display device in accordance with the present invention;

FIGS. **35**A to **35**C each illustrate an example of a peripheral component of a display device in accordance with the present invention;

FIGS. **36**A and **36**B each illustrate an example of a circuit structure of a display device in accordance with the present invention;

FIG. **37** illustrates an example of a circuit structure of a display device in accordance with the present invention;

FIG. **38** illustrates an example of a circuit structure of a display device in accordance with the present invention;

FIGS. **39**A and **39**B each illustrate an example of a cross-sectional view of a display device in accordance with the present invention;

FIGS. **40**A to **40**D each illustrate an example of a cross-sectional view of a display device in accordance with the present invention;

FIGS. **41**A to **41**D each illustrate an example of a cross-sectional view of a display device in accordance with the present invention;

FIGS. **42**A to **42**D each illustrate an example of a cross-sectional view of a display device in accordance with the present invention;

FIG. **43** illustrates an example of a top plan view of a display device in accordance with the present invention;

FIGS. **44**A to **44**D each illustrate an example of a top plan view of a display device in accordance with the present invention;

FIGS. **45**A to **45**D each illustrate an example of a top plan view of a display device in accordance with the present invention;

FIG. **46**A illustrates an example of a pixel layout of a display device in accordance with the present invention, and FIG. **46**B illustrates an example of a cross-sectional view thereof;

FIG. **47**A illustrates an example of a pixel layout of a display device in accordance with the present invention, and FIG. **47**B illustrates an example of a cross-sectional view thereof;

FIG. **48**A illustrates an example of a pixel layout of a display device in accordance with the present invention, and FIG. **48**B illustrates an example of a cross-sectional view thereof;

FIGS. **49**A and **49**B each illustrate an example of a timing chart of a display device in accordance with the present invention;

FIGS. **50**A and **50**B each illustrate an example of a timing chart of a display device in accordance with the present invention;

FIG. **51** illustrates an example of a circuit structure of a display device in accordance with the present invention;

FIG. **52** illustrates an example of a circuit structure of a display device in accordance with the present invention;

FIG. **53** illustrates an example of a circuit structure of a display device in accordance with the present invention;

FIG. **54** illustrates an example of a circuit structure of a display device in accordance with the present invention;

FIG. **55** illustrates an example of a circuit structure of a display device in accordance with the present invention;

FIGS. **56**A to **56**G illustrate a manufacturing process of a display device in accordance with the present invention;

FIG. **57** illustrates an example of a cross-sectional view of a display device in accordance with the present invention;

FIG. **58** illustrates an example of a cross-sectional view of a display device in accordance with the present invention;

FIG. **59** illustrates an example of a cross-sectional view of a display device in accordance with the present invention;

FIG. **60** illustrates an example of a cross-sectional view of a display device in accordance with the present invention;

FIGS. **61**A to **61**C each illustrate an example of a display element of a display device in accordance with the present invention;

FIGS. **62**A to **62**C each illustrate an example of a display element of a display device in accordance with the present invention;

FIGS. **63**A and **63**B illustrate an example of a structure of a display device in accordance with the present invention;

FIG. **64** illustrates an example of a structure of a display device in accordance with the present invention;

FIG. **65** illustrates an example of a structure of a display device in accordance with the present invention;

FIG. **66** illustrates an example of a structure of a display device in accordance with the present invention;

FIGS. **67**A to **67**C each illustrate an example of a structure of a display device in accordance with the present invention;

FIG. **68** illustrates an example of a circuit structure of a display device in accordance with the present invention;

FIG. **69** illustrates an example of a timing chart of a display device in accordance with the present invention;

FIG. **70** illustrates an example of a timing chart of a display device in accordance with the present invention;

FIGS. **71**A and **71**B each illustrate an example of a driving method of a display device in accordance with the present invention;

FIGS. **72**A to **72**E each illustrate an example of a display element of a display device in accordance with the present invention;

FIG. **73** illustrates an example of a manufacturing device of a display device in accordance with the present invention;

FIG. **74** illustrates an example of a manufacturing device of a display device in accordance with the present invention;

FIG. **75** illustrates an example of a structure of a display device in accordance with the present invention;

FIG. **76** illustrates an example of a structure of a display device in accordance with the present invention;

FIGS. **77**A and **77**B each illustrate an example of a structure of a display device in accordance with the present invention;

FIGS. **78**A and **78**B each illustrate an example of a structure of a display device in accordance with the present invention;

FIG. **79** illustrates an example of a structure of a display device in accordance with the present invention;

FIG. **80** illustrates an example of a structure of a display device in accordance with the present invention;

FIGS. **81**A to **81**H each illustrate an electronic device using a display device in accordance with the present invention;

FIG. **82** illustrates an electronic device using a display device in accordance with the present invention;

FIG. **83** illustrates an electronic device using a display device in accordance with the present invention;

FIG. **84** illustrates an electronic device using a display device in accordance with the present invention;

FIG. **85** illustrates an electronic device using a display device in accordance with the present invention;

FIGS. **86**A and **86**B each illustrate an electronic device using a display device in accordance with the present invention; and

FIGS. **87**A and **87**B illustrate an electronic device using a display device in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, the present invention will be described by way of embodiment modes and embodiments with reference to the drawings. However, the present invention can be implemented in various different ways and it will be easily understood by those skilled in the art that various changes and modifications are possible. Unless such changes and modifications depart from the spirit and the scope of the present invention, they should be construed as being included therein. Therefore, the present invention should not be construed as being limited to the description of the embodiment modes and embodiments.

[Embodiment Mode 1]

FIG. **1** is a block diagram of a display device of the present invention. The display device of the present invention includes a pixel portion **100** including a plurality of pixels, a scan line driver circuit **101** which can select a plurality of pixels in each line, and a signal line driver circuit **102** which controls input of a video signal to pixels in a selected line. The signal line driver circuit **102** includes at least a shift register **103**, a sampling circuit **104**, and a plurality of memory circuits. Each memory circuit includes a plurality of memory elements which can store data input to pixels for one line.

FIG. **1** shows an example in which a first latch **105**, a second latch **106**, a third latch **107**, and a fourth latch **108** are used for the plurality of memory circuits. Note that the number of latches used in the display device of the present invention is not limited to four, and the number of latches may be two or three, or may be five or more.

Next, an operation of the signal line driver circuit **102** is described. A clock signal S-CLK and a start pulse signal S-SP are input to the shift register **103**. The shift register **103** generates timing signals, pulses of which are sequentially shifted, in accordance with the clock signal S-CLK and the start pulse signal S-SP, and inputs the timing signals to the sampling circuit **104**. The sampling circuit **104** samples video signals for one line period, which are input to the signal line driver circuit **102**, in accordance with the input timing signal. Then, when the video signals corresponding to each pixel are sampled, the sampled video signal is input in each time to one or a plurality of the first latch **105**, the second latch **106**, the third latch **107**, and the fourth latch **108** in the lower stage.

Note that in this embodiment mode, an example is described in which a sampled video signal is input in each time to the memory circuit in the lower stage without waiting for completion of one line period; however, the present invention is not limited to this structure. After all the video signals for one line period are sampled, the sampled video signals may be input to the memory circuit in the lower stage all at once.

In addition, video signals may be sampled for one pixel at one time serially after completion of sampling of video signals for another pixel, or pixels in one line may be divided into several groups and video signals may be sampled for each pixel corresponding in one group at the same time.

Writing latch signals WS_1 to WS_4 which control writing of data included in a video signal and reading latch signals RS_1 to RS_4 which control reading of stored data are input to the first latch **105**, the second latch **106**, the third latch **107**, and the fourth latch **108**, respectively. Specifically, the writing latch signal WS_1 and the reading latch signal RS_1 are input to the first latch **105**. The writing latch signal WS_2 and the reading latch signal RS_2 are input to the second latch **106**. The writing latch signal WS_3 and the reading latch signal RS_3 are input to the third latch **107**. The writing latch signal WS_4 and the reading latch signal RS_4 are input to the fourth latch **108**.

In accordance with the writing latch signals WS_1 to WS_4, data of video signals for one line period, which are input from the signal line driver circuit **102**, are written to and stored in the first latch **105**, the second latch **106**, the third latch **107**, or the fourth latch **108**. Further, in accordance with the reading latch signals RS_1 to RS_4, the data stored in the first latch **105**, the second latch **106**, the third latch **107**, or the fourth latch **108** is output as a video signal.

Note that although the pixel portion **100** is directly connected to the next stage of the memory circuit in FIG. **1**, the present invention is not limited to this structure. A circuit which processes the video signal output from the first latch **105**, the second latch **106**, the third latch **107**, or the fourth latch **108** can be provided in a previous stage of the pixel portion **100**. Examples of the circuit which performs signal processing include a buffer which can shape a waveform, a level shifter which can amplify amplitude, and a digital/analog converter circuit which can convert a digital signal into an analog signal.

Then, at the same time as inputting a video signal to the pixel portion **100** from one of the first latch **105**, the second latch **106**, the third latch **107**, and the fourth latch **108**, the sampling circuit **104** can sample video signals corresponding to the next line period again. Note that in the present invention, when the same data as the video signal corresponding to the next line period is stored in advance in one of the first latch **105**, the second latch **106**, the third latch **107**, and the fourth latch **108**, sampling of the video signal in the sampling circuit **104** can be stopped.

When sampling is stopped, input of pulses of the clock signal S-CLK and the start pulse signal S-SP to the shift register **103** is stopped, and generation of a pulse of the timing signal in the shift register **103** is stopped. Note that in order to stop the generation of a pulse of the timing signal, only input of a pulse of a clock signal S-CLK to the shift register **103** may be stopped, or only input of the pulses of the start pulse signal S-SP to the shift register **103** may be stopped. When output of pulses of a timing signal from the shift register **103** is stopped, the sampling circuit **104** stops sampling of the video signals. Then, in accordance with the reading latch signals RS_1 to RS_4, the same data as the video signals corresponding to the next line period is input as video signals to the pixel portion **100** from one of the first latch **105**, the second latch **106**, the third latch **107**, and the fourth latch **108**.

Next, a specific operation of the signal line driver circuit **102** is described using the case where pieces of data of video signals input to pixels in a j-th line, a (j+a)th line, and a (j+b)th line of the pixel portion **100** are the same, as an example.

First, as shown in FIG. **2**A, it is assumed that the pixels in the j-th line are selected and data stored in the first latch **105**, for example, is input as video signals to the pixels in the j-th line which is selected. Note that the data of the video signals are written to the first latch **105** through a series of operations in the signal line driver circuit **102** in which the shift register **103** generates a timing signal, and the sampling circuit **104** samples the video signals in accordance with a pulse of the timing signal and inputs the sampled video signals to the first latch **105**. That is, in order to input the video signals to the pixels in the j-th line, the shift register **103**, the sampling circuit **104**, and the first latch **105** are driven in the signal line driver circuit **102**, as shown in FIG. **2**B.

Next, as shown in FIG. **3**A, it is assumed that the pixels in the (j+a)th line is selected. Video signals having the same data as that of the video signals input to the j-th line are input to the pixels in the (j+a)th line which is selected. Accordingly, the data stored in the first latch **105** is input as video signals. Note that data of the video signals have already been written to the first latch **105** before the pixels in the j-th line is selected. Therefore, when the data is stored in the first latch **105** after selection of the pixels in the j-th line finishes, writing of the data to the first latch **105** is not necessarily performed again before the pixels in the (j+a)th line are selected. Thus, in order to input video signals to the pixels in the (j+a)th line, it is acceptable as long as only the first latch **105** is driven in the signal line driver circuit **102**, as shown in FIG. **3**B.

Next, as shown in FIG. **4**A, it is assumed that after the pixel in the (j+a)th line is selected and before the pixel in the (j+b)th line is selected, pixels in a line corresponding to another data is selected, and data stored in the third latch **107**, for example, is input as video signals to the pixels in the line which is selected. Note that the data of the video signals are written to the third latch **107** through a series of operations in the signal line driver circuit **102** in which the shift register **103** generates a timing signal, and the sampling circuit **104** samples the video signals in accordance with a pulse of the timing signal and inputs the sampled video signals to the third latch **107**. That is, in order to input the video signals to the pixels in the line, the shift register **103**, the sampling circuit **104**, and the third latch **107** are driven in the signal line driver circuit **102**, as shown in FIG. **4**B.

Note that in the present invention, the data which has already been written can be continuously stored in the first latch **105** while the pixels in the line corresponding to another data are selected. Accordingly, when the pixels in the (j+b)th line is selected, the data stored in the first latch **105** can be input as video signals to the pixels in the (j+b)th line even after selection of the line corresponding to another data finishes. Thus, in order to input the video signals to the pixels in the (j+b)th line, it is acceptable as long as only the first latch **105** is driven in the signal line driver circuit **102**, similarly in the case of FIG. **3**B.

Next, FIG. **5** shows an example of a timing chart of the clock signal S-CLK and the start pulse signal S-SP which are input to the shift register **103**, the writing latch signals WS_1 to WS_4 and the reading latch signals RS_1 to RS_4 which are input to the first latch **105**, the second latch **106**, the third latch **107**, and the fourth latch **108**, respectively, data (referred to as DATA1) of a video signal output from the sampling circuit **104**, and data (referred to as DATA2) of a video signal input to the pixel portion **100**, using the display device shown in FIG. **1** as an example. Note that FIG. **5** shows the case that when video signals corresponding to each pixel are sampled by the sampling circuit **104**, the sampled video signals are input in each time to the memory circuit in the lower stage without waiting for completion of one line period.

As shown in FIG. **5**, in a line period which appears first, a video signal having data denoted by "A" is output from the sampling circuit **104**. The video signals having the data "A", which is output from the sampling circuit **104**, are written to the first latch **105** in accordance with a pulse of the writing latch signal WS_1. Note that at this time, other latch circuits may be made to be in a state capable of being written by the writing latch signal. Accordingly, the data "A" can be written to a plurality of latch circuits concurrently.

In a line period which appears next, video signals having data denoted by "B" are output from the sampling circuit **104**. The video signals having the data "B", which is output from the sampling circuit **104**, are written to the second latch **106** in accordance with a pulse of the writing latch signal WS_2. The video signals having the data "A" are input to the pixel portion **100** from the first latch **105** in accordance with a pulse of the reading latch signal RS_1.

In a line period which appears next, video signals having data denoted by "C" are output from the sampling circuit **104**. The video signals having the data "C", which is output from the sampling circuit **104**, are written to the third latch **107** in accordance with a pulse of the writing latch signal WS_3. The video signals having the data "B" are input to the pixel portion **100** from the second latch **106** in accordance with a pulse of the reading latch signal RS_2.

In a line period which appears next, video signals having data denoted by "D" are output from the sampling circuit **104**. The video signals having the data "D", which is output from the sampling circuit **104**, are written to the fourth latch **108** in accordance with a pulse of the writing latch signal WS_4. The video signals having the data "C" are input to the pixel portion **100** from the third latch **107** in accordance with a pulse of the reading latch signal RS_3.

In a line period which appears next, input of one or both of the pulses of the clock signal S-CLK and the start pulse signal S-SP to the shift register **103** is stopped. Thus, generation of a timing signal in the shift register **103** is stopped, so that updating of output of the video signals from the sampling circuit **104** is stopped. Further, the video signals having the data "D" are input to the pixel portion **100** from the fourth latch **108** in accordance with a pulse of the reading latch signal RS_4.

In a line period which appears next, input of one or both of the pulses of the clock signal S-CLK and the start pulse signal S-SP to the shift register **103** has been stopped, subsequently to the previous line period. Thus, generation of the timing signal in the shift register **103** is stopped, so that updating of output of the video signals from the sampling circuit **104** is stopped. Further, the video signals having the data "A" are input to the pixel portion **100** from the first latch **105** in accordance with the pulse of the reading latch signal RS_1.

In a line period which appears next, input of one or both of the pulses of the clock signal S-CLK and the start pulse signal S-SP to the shift register **103** has been stopped, subsequently to the previous line period. Thus, generation of the timing signal in the shift register **103** is stopped, so that updating of output of the video signal from the sampling circuit **104** is stopped. Further, the video signals having the data "B" are input to the pixel portion **100** from the second latch **106** in accordance with the pulse of the reading latch signal RS_2.

In a line period which appears next, input of the pulses of the clock signals S-CLK and the start pulse signals S-SP to the shift register **103** is resumed. Thus, generation of the timing signals in the shift register **103** is also resumed, so that the video signals having data denoted by "E" are output from the sampling circuit **104**. The video signals having data "E", which are output from the sampling circuit **104**, are written to the third latch **107** in accordance with the pulses of the writing latch signals WS_3. The video signals having the data "A" are input to the pixel portion **100** from the first latch **105** in accordance with the pulses of the reading latch signals RS_1.

In a line period which appears next, input of one or both of the pulses of the clock signals S-CLK and the start pulse signals S-SP to the shift register **103** is stopped. Thus, generation of the timing signals in the shift register **103** is stopped, so that updating of output of the video signals from the sampling circuit **104** is stopped. Further, the video signals having the data "E" are input to the pixel portion **100** from the third latch **107** in accordance with the pulses of the reading latch signals RS_3.

Note that in FIG. **5**, after data of video signals are written to a memory circuit, the written data is input to the pixel portion **100** as video signals in latter periods; however, the present invention is not limited to this configuration. At the same time as writing data of video signals to a memory circuit, the written data may be input to the pixel portion **100** as video signals.

In addition, FIG. **5** illustrates the case that when a video signal corresponding to each pixel is sampled by the sampling circuit **104**, the sampled video signal is input in each time to the memory circuit in the lower stage without waiting for completion of one line period; however, the present invention is not limited to this structure. After all the video signals for one line period are sampled, the sampled video signals may be input to the memory circuit in the lower stage all at once. Note that in this case, the sampling circuit **104** is operated by dividing one line period into a period for sampling video signals and a period for outputting the sampled video signals. Then, the sampled video signals are written to the memory circuit only in the latter period.

Since the display device of the present invention includes a plurality of memory circuits in the signal line driver circuit **102**, pieces of data of video signals corresponding to a plurality of line periods can be concurrently held. Thus, as shown in FIG. **5**, for example, the data "A" and another data can be held in different memory circuits even when a line period corresponding to writing of another data exists during second, sixth, and eighth line periods corresponding to writing of the data "A". Accordingly, in the memory circuit in which the corresponding data "A" is stored (in FIG. **5**, the first latch **105**), it is not necessary to rewrite data until all the second, sixth, and eighth line periods end. That is, input of video signals to the signal line driver circuit **102**, sampling of the video signal in the signal line driver circuit **102**, and writing of data "A" of the sampled video signals can be completed at one time during the second, sixth, and eighth line periods.

Accordingly, in the present invention, power consumption of the signal line driver circuit **102** can be efficiently suppressed even when a plurality of line periods where pieces of data correspond to each other exist discontinuously. Further, power consumption needed for inputting video signals to the signal line driver circuit **102** can be suppressed, so that power consumption of the display device as a whole can be suppressed.

In addition, since the display device of the present invention includes a plurality of memory circuits in the driver circuit, even when a plurality of groups formed of a plurality of line periods where pieces of data correspond to each other exist, for example, a group formed of the second, sixth, and eighth line periods corresponding to the data "A" and a group formed of third, seventh, and tenth line periods corresponding to the data "B", data corresponding to each group can be held in different memory circuits. Accordingly, in the memory circuits in which the data is held, it is not necessary to rewrite the data until all of the line periods in the group corresponding to the data end. That is, input of a video signal to the signal line driver circuit **102**, sampling of the video signal in the signal line driver circuit **102**, and writing of data "A" of the sampled video signal can be completed at one time during the line periods in one group.

Accordingly, power consumption of the signal line driver circuit can be efficiently suppressed even when a plurality of groups each formed of a plurality of line periods where pieces of data correspond to each other exist. Further, power consumption needed for inputting video signals to the signal line driver circuit can be suppressed, so that power consumption of the display device as a whole can be suppressed.

Note that FIG. **5** illustrates the case where two groups, for example, the group formed of a plurality of line periods corresponding to the data "A" and the group formed of a plurality of line periods corresponding to the data "B" exist; however, the number of groups is not limited to two. The number of memory circuits is set as appropriate in accordance with the number of groups in which writing of data to the memory circuits should be omitted and timing of writing and reading data in the memory circuit.

The case as shown in FIG. **5**, for example, is considered in which there is a gap between timing of writing data of a video signal and timing of reading the data. In this case, line sequential driving in which data is written to all pixels belonging to one line all at once can be performed. Further, in this case, when a plurality of line periods, for example, a line period corresponding to the data "C" and a line period corresponding to the data "D", each having data which does not correspond to that of the other line periods, continuously appear, a memory circuit for writing non-corresponding data is necessary in addition to a memory circuit for writing corresponding data. Accordingly, the number of memory circuits provided in the signal line driver circuit is preferably the number obtained by adding one to the number of groups.

Alternatively, a structure which is different from FIG. **5**, for example, may be employed in which data of a video signal is not written to a memory circuit but input as a video signal to the pixel portion **100** directly from the sampling circuit. In this case, dot sequential driving in which a signal is sequentially written to each pixel can be performed. At this time, the signal line driver circuit **102** is not necessarily provided with a memory circuit for writing non-corresponding data, and it is acceptable as long as the signal line driver circuit **102** is provided with a memory circuit for writing corresponding data. Accordingly, in this case, the number of memory circuits provided in the signal line driver circuit **102** is preferably the same as the number of groups.

Note that the signal line driver circuit **102** may be controlled so as to write data of a video signal to a memory circuit and input the written data as a video signal to the pixel portion **100** at the same time, which is different from FIG. **5**. In this case, both writing and reading of data to/from the memory circuit can be performed in one line period. Accordingly, in a structure capable of performing line sequential driving, the signal line driver circuit **102** can perform dot sequential driving.

As the number of memory circuits is increased, the number of writing of data to the memory circuits can be further reduced, which leads to reduction in power consumption of the signal line driver circuit. On the other hand, by suppressing the number of memory circuits, a ratio of the area of a substrate occupied by the signal line driver circuit can be decreased.

In addition, this embodiment mode shows a display device including one signal line driver circuit and one scan line driver circuit; however, the present invention is not limited to this structure. Two or more signal line driver circuits may be provided, or two or more scan line driver circuits may be provided.

When a plurality of signal line driver circuits are provided, sampling of video signals can be sequentially performed by the plurality of signal line driver circuits. Thus, driving frequency of the signal line driver circuits can be reduced, and power consumption can also be reduced. When a plurality of scan line driver circuits are provided, a plurality of lines can be selected at the same time and pieces of data can be concurrently written; thus, one line period can be extended. Accordingly, since driving frequency of the signal line driver circuit can be reduced, power consumption can also be reduced.

Note that although this embodiment mode is described with reference to various drawings, the contents (or part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in another drawing. Further, much more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or part of the contents) described in each drawing in this embodiment mode can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in a drawing in another embodiment mode or embodiment. Further, much more drawings can be formed by combining each part in each drawing in this embodiment mode with part of another embodiment mode or embodiment.

Note that this embodiment mode shows examples of embodying, slightly transforming, partially modifying, improving, describing in detail, or applying the contents (or part of the contents) described in other embodiment modes and embodiments, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment mode.

[Embodiment Mode 2]

FIG. **6** is a block diagram of a display device of the present invention. The display shown in FIG. **6** includes a memory for storing video signals and a data comparison portion **110** which compares video signals stored in the memory in corresponding line periods in addition to the display device shown in FIG. **1**. FIG. **6** shows an example in which a RAM (random access memory) **111** and a RAM **112** are used as the memory for storing the video signals. For the RAMs **111** and **112**, various RAMs such as an SDRAM (synchronous dynamic random access memory), a DRAM (dynamic random access memory), and an SRAM (static random access memory) can be used.

In addition, the display device of the present invention may include a control circuit **113** and a data format circuit **114** as shown in FIG. **6**. A clock signal CLK and a signal which is used for reconstructing a screen in the pixel portion **100**, such as a horizontal synchronization signal Hsync used for horizontal synchronization or a vertical synchronization signal Vsync used for vertical synchronization are input to the control circuit **113**. The control circuit **113** can generate the clock signal S-CLK and the start pulse signal S-SP for controlling operation of the signal line driver circuit **102**, and a clock signal G-CLK and a start pulse signal G-SP for controlling operation of the scan line driver circuit **101** by using the input signals.

The data format circuit **114** can generate a video signal which meets specifications of the pixel portion **100**, the scan line driver circuit **101**, and the signal line driver circuit **102** in accordance with the signal from the control circuit **113** by using input image data.

The video signal output from the data format circuit **114** is stored in the RAM **111** or the RAM **112**. This embodiment mode describes the case where video signals corresponding to one frame period is stored in each of the RAM **111** and the RAM **112**; however, the present invention is not limited to this structure. Video signals corresponding to a period longer than one frame period or video signals corresponding to a period shorter than one frame period may be stored in each of the RAM **111** and the RAM **112**.

In addition, this embodiment mode shows an example in which two RAMs are used for the memories; however, the number of memories is not limited to two in the present invention. For example, video signals may be stored in three or more memories, or one memory. Note that when a plurality of memories are employed, writing of video signals to the memories and reading of video signals from the memories can be performed at the same time, so that driving speed of the data comparison portion **110** can be further increased. Thus, comparison of much more data can be performed, and power consumption can be more efficiently suppressed.

Information on corresponding line periods is added to the video signals stored in the RAM **111** and the RAM **112** by the data format circuit **114**. The data comparison portion **110** reads pieces of data of the video signals corresponding to respective line periods from the RAM **111** or the RAM **112**, compares the pieces of data, and extracts a plurality of line periods where pieces of data correspond to each other. Then, the data comparison portion **110** generates the writing latch signals WS_1 to WS_4 so that the corresponding data is written to one of memory circuits in accordance with timing of a line period which appears first among the plurality of line periods and the data written to the memory circuits is stored in the memory circuits until a line period which appears last among the plurality of line periods ends. Further, the data comparison portion **110** generates the reading latch signals RS_1 to RS_4 so that the data written to the memory circuits are input as video signals to the pixel portion **100** in a plurality of line periods where pieces of data correspond to each other. The writing latch signals WS_1 to WS_4 and the reading latch signals RS_1 to RS_4 which are generated are input from the data comparison portion **110** to the memory circuits in the signal line driver circuit **102**.

In addition, the data comparison portion **110** processes the start pulse signal S-SP and the clock signal S-CLK input to the data comparison portion **110** so that output of pulses is stopped in a period during which writing is preformed in a plurality of lines in accordance with timing at which a plurality of line periods appear so that sampling of video signals in the signal line driver circuit **102** can be completed at one time since the first line period appears and until the last line period ends through, in other words, in the plurality of line periods where pieces of data of video signals correspond to each other. Then, the data comparison portion **110** inputs the processed start pulse signal S-SP and the clock signal S-CLK to the shift register **103** in the signal line driver circuit **102**. With the aforementioned structure, sampling of video signals in the sampling circuit **104** can be performed just once during the plurality of line periods.

Further, the data comparison portion **110** controls output of video signals in accordance with timing at which the plurality of line periods appear so that input of video signals to the signal line driver circuit **102** can be completed at one time during the plurality of line periods where pieces of data of video signals correspond to each other.

FIG. **7** shows an example of a specific structure of the data comparison portion **110**. In a block diagram shown in FIG. **7**, the data comparison portion **110** includes a comparator **115**, an address memory **116**, an arithmetic circuit **117**, a PLL (phase locked loop) circuit **118**, and a signal control circuit **119**.

The arithmetic circuit **117** reads a video signal from the RAM **111** or the RAM **112**. For example, it is assumed that the arithmetic circuit **117** reads video signals in a j-th line period and video signals in a (j+a)th line period. The arithmetic circuit **117** controls the comparator **115** so as to compare pieces of data of the read video signals. When the pieces of data of the video signals correspond to each other as a result of comparison by the comparator **115**, the arithmetic circuit **117** makes the address memory **116** store information on line periods the pieces of data of which correspond to each other.

The arithmetic circuit **117** needs to be driven at higher speed as the number of line periods in which pieces of data should be compared is increased. For example, when data corresponding to one line period is compared with data corresponding to N pieces of line periods, the frequency of a clock signal controlling driving of the arithmetic circuit **117** is preferably N times the frequency of the clock signal S-CLK. Accordingly, in the data comparison portion **110** shown in FIG. **7**, the frequency of the input clock signals S-CLK is converted into N times by the PLL circuit **118** and the clock signals S-CLK with the converted frequency are input to the arithmetic circuit **117**.

Note that a clock signal for controlling driving of the arithmetic circuit **117** may be separately generated in the control circuit **113**, which is not shown in FIG. **7**, and input to the arithmetic circuit **117**. In this case, the frequency of the clock signal for controlling driving of the arithmetic circuit **117** can be controlled by the control circuit **113**; thus, the PLL circuit **118** is not necessarily provided.

Further, the arithmetic circuit **117** reads information on line periods the pieces of data of which correspond to each other from the address memory **116**. Then, the arithmetic circuit **117** controls the signal control circuit **119** so that the start pulse signal S-SP and the clock signal S-CLK which are input to the data comparison portion **110** are processed in accordance with timing at which the line periods appear. The processed start pulse signal S-SP and clock signal S-CLK are input from the signal control circuit **119** to the signal line driver circuit **102**.

Moreover, the arithmetic circuit **117** controls the signal control circuit **119** so that the writing latch signals WS_1 to WS_4 and the reading latch signals RS_1 to RS_4 are generated in accordance with the timing at which the line periods appear. The generated writing latch signals WS_1 to WS_4 and reading latch signals RS_1 to RS_4 are input from the signal control circuit **119** to the signal line driver circuit **102**.

Furthermore, the arithmetic circuit **117** controls input of video signals from the signal control circuit **119** to the signal line driver circuit **102** in accordance with the timing at which the line periods appear. For example, as shown in FIG. **7**, in the j-th line period, video signals in the j-th line period and video signals in a (j+p)th line period are input to the arithmetic circuit **117** and pieces of data are compared. Then, regardless of the result of comparison, the arithmetic circuit **117** controls the signal control circuit **119** so that the video signals in the j-th line period are output to the signal line driver circuit **102**. Next, as shown in FIG. **21**, when the data of the video signals in the j-th line period and the data of the video signals in the (j+p)th line period correspond to each other, the arithmetic circuit **117** stops output of the video signals to the signal line driver circuit **102** in the (j+p)th line period. On the other hand, when the data of the video signals in the j-th line period and the data of the video signals in the (j+p)th line period do not correspond to each other, the arithmetic circuit **117** controls the signal control circuit **119** so that the video signals in the (j+p)th line period is output to the signal line driver circuit **102**. Note that in the (j+p)th line period, the video signals in the (j+p)th line period and video signals in a (j+q)th period ($p<q$) are input to the arithmetic circuit **117** and pieces of data are compared.

Note that the case is assumed in which a plurality of groups each including a plurality of line periods corresponding to the same data exist and the number of groups is larger than the number of memory circuits which can store data. In this case, a group in which data is written to a memory circuit earlier may be preceded, and in the other groups, a normal operation, that is, rewriting of data of video signals in the memory circuit may be performed in each line period. Alternatively, even when another data has been written to the memory circuit earlier and a line period belonging to another group appears later, data corresponding to another group may be written so that the group is preceded.

Alternatively, data of a group in which the number of line periods corresponding to the same data is large may be written to the memory circuit so that the group is preceded. FIG. **8** shows a structure of the data comparison portion **110** in the case where a plurality of groups each including a plurality of line periods corresponding to the same data exist and priority is given to the groups in accordance with the number of line periods.

In a block diagram shown in FIG. **8**, the data comparison portion **110** includes a counter **120** in addition to the comparator **115**, the address memory **116**, the arithmetic circuit **117**, the PLL (phase locked loop) circuit **118**, and the signal control circuit **119**. In the data comparison portion **110** shown in FIG. **8**, when pieces of data correspond to each other as a result of comparison in the comparator **115**, information on the fact that the pieces of data correspond to each other is transmitted to the counter **120**. When the counter **120** counts the number of line periods where pieces of data correspond to each other based on the information, the arithmetic circuit **117** sets priorities to each group in accordance with the number of line periods. Then, the arithmetic circuit **117** controls the signal control circuit **119** so that the signal control circuit **119** generates the writing latch signals WS_1 to WS_4 and the reading latch signals RS_1 to RS_4 in order that data of a group more highly preceded is preferentially stored in a memory circuit.

Note that in the display device of the present invention shown in FIG. **6**, signal processing of the start pulse signal S-SP and the clock signal S-CLK and generation of the writing latch signals WS_1 to WS_4 and the reading latch signals RS_1 to RS_4 are all performed in the data comparison portion **110**; however, these operations may be performed in the control circuit **113**. Next, an operation of the data comparison portion **110** in the display device shown in FIG. **6** is described with reference to FIG. **9** in the case where signal processing of the start pulse signal S-SP and the clock signal S-CLK and generation of the writing latch signals WS_1 to WS_4 and the reading latch signals RS_1 to RS_4 are performed in the control circuit **113**.

In a block diagram shown in FIG. **9**, the data comparison portion **110** reads pieces of data of video signals corresponding to each line period from the RAM **111** or the RAM **112**, compares the pieces of data, and extracts a plurality of line periods where pieces of data of video signals correspond to each other. Then, a signal including information on which line periods are extracted is input to the control circuit **113** as a timing control signal. Further, the data comparison portion **110** controls output of video signals in accordance with timing at which the plurality of line periods appear so that input of video signals to the signal line driver circuit **102** can be completed at one time during the plurality of line periods where the pieces of data of video signals correspond to each other.

The control circuit **113** generates the writing latch signals WS_1 to WS_4 in accordance with the input timing control signal so that the corresponding data is written to one of memory circuits in accordance with timing of a line period which appears first among the plurality of line periods where the pieces of data correspond to each other and the data written to the memory circuit is stored in the memory circuit until a line period which appears last among the plurality of line periods ends. Further, the control circuit **113** generates the reading latch signals RS_1 to RS_4 in accordance with the timing control signal input thereto so that the data written to the memory circuit is input as video signals to the pixel portion **100** in the plurality of line periods where the pieces of data correspond to each other. The writing latch signals WS_1 to WS_4 and reading latch signals RS_1 to RS_4 which are generated are input from the control circuit **113** to the memory circuit in the signal line driver circuit **102**.

The clock signal CLK and a signal used for reconstructing a screen in the pixel portion **100**, such as the horizontal synchronization signal Hsync used for horizontal synchronization or the vertical synchronization signal Vsync used for vertical synchronization are input to the control circuit **113**. The control circuit **113** can generate the clock signal S-CLK and the start pulse signal S-SP for controlling the operation of the signal line driver circuit **102**, the clock signal G-CLK and the start pulse signal G-SP for controlling the operation of the scan line driver circuit **101**, and a clock signal A-CLK for controlling the driving of the data comparison portion **110** by using the input signals. The clock signal A-CLK is output from the control circuit **113** to the data comparison portion **110**. The control circuit **113** processes the start pulse signal S-SP and the clock signal S-CLK in accordance with the input timing control signal so that sampling of video signals in the signal line driver circuit **102** can be completed at one time during a plurality of line periods where pieces of data of video signals correspond to each other, and inputs the processed start pulse signal S-SP and clock signal S-CLK to the shift register **103** in the signal line driver circuit **102**. With the aforementioned structure, sampling of video signals in the sampling circuit **104** can be performed just once through a plurality of line periods.

Next, an operation of the data comparison portion **110** shown in FIGS. **7** and **8** is described with reference to FIG. **10** in the case where signal processing of the start pulse signal S-SP and the clock signal S-CLK and generation of the writing latch signals WS_1 to WS_4 and the reading latch signals RS_4 to RS_4 are performed in the control circuit **113**. Note that FIG. **10** shows the operation of the data comparison portion **110** shown in FIG. **8** as an example; however, the operation of the data comparison portion **110** shown in FIG. **7** can be similarly described.

In FIG. **10**, the arithmetic circuit **117** reads information on line periods where the pieces of data correspond to each other from the address memory **116**. Then, the arithmetic circuit **117** controls the signal control circuit **119** so that the signal control circuit **119** generates a timing control signal including information on which line periods are extracted based on the information. The generated timing control signal is input from the signal control circuit **119** to the control circuit **113**.

Further, in the data comparison portion **110** shown in FIG. **10**, the frequency of the input clock signal A-CLK is converted into N times by the PLL circuit **118** and the input clock signal A-CLK with the converted frequency is input to the arithmetic circuit **117**. The frequency of the clock signal A-CLK for controlling the driving of the arithmetic circuit **117** may be separately converted by the control circuit **113** and the input clock signal A-CLK with the converted frequency is input to the arithmetic circuit **117**. In this case, the frequency of the clock signal for controlling the driving of the arithmetic circuit **117** is controlled by the control circuit **113**; thus, the PLL circuit **118** is not necessarily provided.

In the display device of the present invention, data of video signals corresponding to a plurality of line periods or a plurality of frame periods is stored in the RAM **111** and the RAM **112**; thus, the data comparison portion **110** can compare data of video signals corresponding to one line period with data of video signals corresponding to other line periods. Accordingly, comparison of not only pieces of data corresponding to adjacent line periods but also pieces of data corresponding to much more line periods can be performed, so that power consumption of the signal line driver circuit **102** can be efficiently suppressed.

Note that although this embodiment mode is described with reference to various drawings, the contents (or part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in another drawing. Further, much more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or part of the contents) described in each drawing in this embodiment mode can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in a drawing in another embodiment mode or embodiment. Further, much more drawings can be formed by combining each part in each drawing in this embodiment mode with part of another embodiment mode or embodiment.

Note that this embodiment mode shows examples of embodying, slightly transforming, partially modifying, improving, describing in detail, or applying the contents (or part of the contents) described in other embodiment modes and embodiments, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment mode.

[Embodiment Mode 3]

In this embodiment mode, a structure of a scan line driver circuit included in a display device of the present invention is described. FIG. **11** shows a block diagram of a structure of the display device of the present invention as an example. FIG. **11** shows a more detailed structure of the scan line driver circuit **101** in the display device shown in FIG. **1**. In FIG. **11**, the scan line driver circuit **101** includes a shift register **121** and a buffer **122**.

The start pulse signal G-SP and the clock signal G-CLK are input to the scan line driver circuit **101**. The shift register **103** generates selection signals, pulses of which are sequentially shifted, in accordance with the start pulse signal G-SP and the clock signal G-CLK. The buffer **122** shapes waveforms of the generated selection signal or amplifies the generated selection signal and inputs the signal to the pixel portion **100**. The selection signals are input to pixels in each line, and one line can be selected from a plurality of lines by the pulses of the selection signals.

Note that waveform shaping corresponds to controlling the pulse width by a logic circuit using a logic element such as an AND gate, an OR gate, a NAND gate, or a NOR gate. In addition, amplification corresponds to changing amplitude of a signal by using a level shifter, a differential amplifier circuit, or the like, and impedance matching with a wiring in the pixel portion due to size adjustment or the like of a transistor.

A video signal is input from the signal line driver circuit **102** to pixels in the selected line.

The contents (or part of the contents) described in each drawing in this embodiment mode can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in a drawing in another embodiment mode or embodiment. Further, much more drawings can be formed by combining each part in each drawing in this embodiment mode with part of another embodiment mode or embodiment.

Note that this embodiment mode shows examples of embodying, slightly transforming, partially modifying, improving, describing in detail, or applying the contents (or part of the contents) described in other embodiment modes and embodiments, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment mode.

[Embodiment Mode 4]

In this embodiment mode, a structure of a display device of the present invention is described in which an analog video signal is input to a pixel portion. FIG. **12** shows a diagram of a structure of the display device of the present invention as an example.

The display device of the present invention shown in FIG. **12** includes a pixel portion **200** including a plurality of pixels, a scan line driver circuit **201** which can select a plurality of pixels in each line, and a signal line driver circuit **202** which controls input of a video signal to pixels in a selected line. The signal line driver circuit **202** includes at least a shift register **203**, a sampling circuit **204**, a plurality of memory circuits, and a digital/analog (D/A) converter circuit **209**. FIG. **12** shows an example in which a first latch **205**, a second latch **206**, a third latch **207**, and a fourth latch **208** are used for the plurality of memory circuits. Note that the number of latches used in the display device of the present invention is not limited to four, and the number of latches may be two or three, or may be five or more.

Next, an operation of the signal line driver circuit **202** is described. In the display device shown in FIG. **12**, the clock signal S-CLK and the start pulse signal S-SP are input to the shift register **203**, similarly to the case of FIG. **1**. The shift register **203** generates timing signals, pulses of which are sequentially shifted, in accordance with the clock signal S-CLK and the start pulse signal S-SP and inputs the timing signal to the sampling circuit **204**. The sampling circuit **204** samples video signals for one line period, which are input to the signal line driver circuit **202**, in accordance with the input timing signal. Then, when all the video signals for one line period are sampled, the sampled video signals are output all at once to one or a plurality of the first latch **205**, the second latch **206**, the third latch **207**, and the fourth latch **208**.

Note that in this embodiment mode, an example is described in which all the video signals for one line period are sampled and thereafter, the sampled video signals are input all at once to the memory circuit in the lower stage; however, the present invention is not limited to this structure. A video signal corresponding to each pixel may be sampled and input in each time to the memory circuit in the lower stage without waiting for completion of one line period.

In addition, video signals may be sampled sequentially in corresponding pixels, or pixels in one line may be divided into several groups and video signals may be sampled in each pixel corresponding to each group at the same time.

In this embodiment mode, the number of memory elements included in each memory circuit is determined in accordance with the number of bits of a digital video signal to be input. For example, when display is performed with an 8-bit video signal, each of the first latch **205**, the second latch **206**, the third latch **207**, and the fourth latch **208** includes flip-flop circuits which are eight times the number of pixels included in one line.

The writing latch signals WS_1 to WS_4 which control writing of data included in the video signal and the reading latch signals RS_1 to RS_4 which control reading of stored data are input to the first latch **205**, the second latch **206**, the third latch **207**, and the fourth latch **208**, respectively. Specifically, the writing latch signal WS_1 and the reading latch signal RS_1 are input to the first latch **205**. The writing latch signal WS_2 and the reading latch signal RS_2 are input to the second latch **206**. The writing latch signal WS_3 and the reading latch signal RS_3 are input to the third latch **207**. The writing latch signal WS_4 and the reading latch signal RS_4 are input to the fourth latch **208**.

In accordance with the writing latch signals WS_1 to WS_4, data of video signals for one line period, which are output from the signal line driver circuit **202**, are written to and stored in the first latch **205**, the second latch **206**, the third latch **207**, or the fourth latch **208**. Further, in accordance with the reading latch signals RS_1 to RS_4, the data stored in the first latch **205**, the second latch **206**, the third latch **207**, or the fourth latch **208** is input to as a video signal to the D/A converter circuit **209**. The D/A converter circuit **209** converts the input digital video signal into an analog video signal and inputs the analog video signal to the pixel portion **200**.

Note that although the pixel portion **200** is directly connected to the next stage of the D/A converter circuit **209** in FIG. **12**, the present invention is not limited to this structure. A circuit which processes the analog video signal output from the D/A converter circuit **209** can be provided in a previous stage of the pixel portion **200**. Examples of the circuit which performs signal processing include a buffer which can shape a waveform and a level shifter which can amplify amplitude.

Then, at the same time as inputting a video signal to the pixel portion **200** from the D/A converter circuit **209**, the sampling circuit **204** can sample a video signal corresponding to the next line period again. Note that in the present invention, when the same data as the video signal corresponding to the next line period is stored in advance in one of the first latch **205**, the second latch **206**, the third latch **207**, and the fourth latch **208**, sampling of the video signal in the sampling circuit **204** can be stopped.

When sampling is stopped, input of pulses of one or both of the clock signal S-CLK and the start pulse signal S-SP to the shift register **203** is stopped, and generation of a pulse of the timing signal in the shift register **203** is stopped. When output of the pulse of the timing signal from the shift register **203** is stopped, the sampling circuit **204** stops sampling of the video signal. Then, in accordance with the reading latch signals RS_1 to RS_4, the same data as the video signal corresponding to the next line period is input as a video signal to the D/A converter circuit **209** from one of the first latch **205**, the second latch **206**, the third latch **207**, and the fourth latch **208**. The D/A converter circuit **209** converts the input digital video signal into an analog video signal and inputs the analog video signal to the pixel portion **200**.

As shown in this embodiment mode, in the display device of the present invention, a display element included in the pixel of the pixel portion **200** can perform display using an analog video signal.

The contents (or part of the contents) described in each drawing in this embodiment mode can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in a drawing in another embodiment mode or embodiment. Further, much more drawings can be formed by combining each part in each drawing in this embodiment mode with part of another embodiment mode or embodiment.

Note that this embodiment mode shows examples of embodying, slightly transforming, partially modifying, improving, describing in detail, or applying the contents (or part of the contents) described in other embodiment modes and embodiments, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment mode.

[Embodiment Mode 5]

In this embodiment mode, a pixel structure of a display device is described. In particular, a pixel structure of a liquid crystal display device is described.

A pixel structure in the case where each liquid crystal mode and a transistor are combined is described with reference to cross-sectional views of a pixel.

Note that as the transistor, a thin film transistor (a TFT) or the like including a non-single crystalline semiconductor layer typified by amorphous silicon, polycrystalline silicon, micro crystalline (also referred to as semi-amorphous) silicon, or the like can be used.

As a structure of the transistor, a top-gate structure, a bottom-gate structure, or the like can be used. Note that a channel-etched transistor, a channel-protective transistor, or the like can be used as a bottom-gate transistor.

FIG. **22** is an example of a cross-sectional view of a pixel in the case where a TN mode and a transistor are combined. By applying the pixel structure shown in FIG. **22** to a liquid crystal display device, a liquid crystal display device can be formed at low cost.

Features of the pixel structure shown in FIG. **22** are described. Liquid crystal molecules **10118** shown in FIG. **22** are long and narrow molecules each having a major axis and a minor axis. In FIG. **22**, a direction of each of the liquid crystal molecules **10118** is expressed by the length thereof. That is, the direction of the major axis of the liquid crystal molecule **10118**, which is expressed as long, is parallel to the page, and as the liquid crystal molecule **10118** is expressed to be shorter, the direction of the major axis becomes closer to a normal direction of the page. That is, among the liquid crystal molecules **10118** shown in FIG. **22**, the direction of the major axis of the liquid crystal molecule **10118** which is close to the first substrate **10101** and the direction of the major axis of the liquid crystal molecule **10118** which is close to the second substrate **10116** are different from each other by 90 degrees, and the directions of the major axes of the liquid crystal molecules **10118** located therebetween are arranged so as to link the above two directions smoothly. That is, the liquid crystal molecules **10118** shown in FIG. **22** are aligned to be twisted by 90 degrees between the first substrate **10101** and the second substrate **10116**.

Note that the case is described in which a bottom-gate transistor using an amorphous semiconductor is used as the transistor. In the case where a transistor using an amorphous semiconductor is used, a liquid crystal display device can be formed at low cost by using a large substrate.

A liquid crystal display device includes a basic portion displaying images, which is called a liquid crystal panel. The liquid crystal panel is manufactured as follows: two processed substrates are attached to each other with a gap of several μm therebetween, and a liquid crystal material is injected into a space between the two substrates, In FIG. **22**, the two substrates correspond to the first substrate **10101** and the second substrate **10116**. A transistor and a pixel electrode are formed over the first substrate. A light-shielding film **10114**, a color filter **10115**, a fourth conductive layer **10113**, a spacer **10117**, and a second alignment film **10112** are formed on the second substrate.

The light-shielding film **10114** is not necessarily formed on the second substrate **10116**. When the light-shielding film **10114** is not formed, the number of steps is reduced, so that manufacturing cost can be reduced. In addition, since a structure is simple when the light-shielding film **10114** is not formed, yield can be improved. Alternatively, when the light-shielding film **10114** is formed, a display device with little light leakage at the time of black display can be obtained.

The color filter **10115** is not necessarily formed on the second substrate **10116**. When the color filter **10115** is not formed, the number of steps is reduced, so that manufacturing cost can be reduced. In addition, since a structure is simple when the color filter **10115** is not formed, yield can be improved. Note that even when the color filter **10115** is not formed, a display device which can perform color display can be obtained by field sequential driving. Alternatively, when the color filter **10115** is formed, a display device which can perform color display can be obtained.

Spherical spacers may be dispersed on the second substrate **10116** instead of forming the spacer **10117**. When the spherical spacers are dispersed, the number of steps is reduced, so that manufacturing cost can be reduced. In addition, since a structure is simple when the spherical spacers are dispersed, yield can be improved. Alternatively, when the spacer **10117** is formed, a distance between the two substrates can be uniform because a position of the spacer is not varied, so that a display device with little display unevenness can be obtained.

A process to be performed to the first substrate **10101** is described.

First, a first insulating film **10102** is formed over the first substrate **10101** by sputtering, a printing method, a coating method, or the like. Note that the first insulating film **10102** is not necessarily formed. The first insulating film **10102** has a function of preventing change in characteristics of the transistor due to an impurity from the first substrate **10101** which affects a semiconductor layer.

Next, a first conductive layer **10103** is formed over the first insulating film **10102** by photolithography, a laser direct writing method, an inkjet method, or the like.

Next, a second insulating film **10104** is formed over the entire surface by sputtering, a printing method, a coating method, or the like. The second insulating film **10104** has a function of preventing change in characteristics of the transistor due to an impurity from the first substrate **10101** which affects the semiconductor layer.

Next, a first semiconductor layer **10105** and a second semiconductor layer **10106** are formed. Note that the first semiconductor layer **10105** and the second semiconductor layer **10106** are formed sequentially and shapes thereof are processed at the same time.

Next, a second conductive layer **10107** is formed by photolithography, a laser direct writing method, an inkjet method, or the like. Note that as a method for etching which is performed at the time of processing a shape of the second conductive layer **10107**, dry etching is preferable. Note that either a light-transmitting material or a reflective material may be used for the second conductive layer **10107**.

Next, a channel formation region of the transistor is formed. Here, an example of a step thereof is described. The second semiconductor layer **10106** is etched by using the second conductive layer **10107** as a mask. Alternatively, the second semiconductor layer **10106** is etched by using a mask for processing the shape of the second conductive layer **10107**. Then, the first conductive layer **10103** at a position where the second semiconductor layer **10106** is removed serves as the channel formation region of the transistor. Thus, the number of masks can be reduced, so that manufacturing cost can be reduced.

Next, a third insulating film **10108** is formed and a contact hole is selectively formed in the third insulating film **10108**. Note that a contact hole may be formed also in the second insulating film **10104** at the same time as forming the contact hole in the third insulating film **10108**. Note that a surface of the third insulating film **10108** is preferably as even as possible. This is because alignment of the liquid crystal molecules are affected by unevenness of a surface with which the liquid crystal is in contact.

Next, a third conductive layer **10109** is formed by photolithography, a laser direct writing method, an inkjet method, or the like.

Next, a first alignment film **10110** is formed. Note that after the first alignment film **10110** is formed, rubbing may be performed so as to control the alignment of the liquid crystal molecules. Rubbing is a step of forming stripes on an alignment film by rubbing the alignment film with a cloth. By performing rubbing, the alignment film can have alignment properties.

The first substrate **10101** which is manufactured as described above and the second substrate **10116** on which the light-shielding film **10114**, the color filter **10115**, the fourth conductive layer **10113**, the spacer **10117**, and the second alignment film **10112** are formed are attached to each other by a sealant with a gap of several μm therebetween. Then, a liquid crystal material is injected into a space between the two substrates. Note that in the TN mode, the fourth conductive layer **10113** is formed over the entire surface of the second substrate **10116**.

FIG. **23**A is an example of a cross-sectional view of a pixel in the case where an MVA (multi-domain vertical alignment) mode and a transistor are combined. By applying the pixel structure shown in FIG. **23**A to a liquid crystal display device, a liquid crystal display device having a wide viewing angle, high response speed, and high contrast can be obtained.

Features of the pixel structure shown in FIG. **23**A are described. Liquid crystal molecules **10218** shown in FIG. **23**A are long and narrow molecules each having a major axis and a minor axis. In FIG. **23**A, a direction of each of the liquid crystal molecules **10218** is expressed by the length thereof. That is, the direction of the major axis of the liquid crystal molecule **10218**, which is expressed as long, is parallel to the page, and as the liquid crystal molecule **10218** is expressed to be shorter, the direction of the major axis becomes closer to a normal direction of the page. That is, each of the liquid crystal molecules **10218** shown in FIG. **23**A is aligned such that the direction of the major axis is normal to the alignment film. Thus, the liquid crystal molecules **10218** at a position where an alignment control protrusion **10219** is formed are aligned radially with the alignment control protrusion **10219** as a center. With this state, a liquid crystal display device having a wide viewing angle can be obtained.

Note that the case is described in which a bottom-gate transistor using an amorphous semiconductor is used as the transistor. In the case where a transistor using an amorphous semiconductor is used, a liquid crystal display device can be formed at low cost by using a large substrate.

A liquid crystal display device includes a basic portion displaying images, which is called a liquid crystal panel. The liquid crystal panel is manufactured as follows: two processed substrates are attached to each other with a gap of several μm therebetween, and a liquid crystal material is injected into a space between the two substrates. In FIG. **23**A, the two substrates correspond to the first substrate **10201** and the second substrate **10216**. A transistor and a pixel electrode are formed over the first substrate. A light-shielding film **10214**, a color filter **10215**, a fourth conductive layer **10213**, a spacer **10217**, a second alignment film **10212**, and an alignment control protrusion **10219** are formed on the second substrate.

The light-shielding film **10214** is not necessarily formed on the second substrate **10216**. When the light-shielding film **10214** is not formed, the number of steps is reduced, so that manufacturing cost can be reduced. In addition, since a structure is simple when the light-shielding film **10214** is not formed, yield can be improved. Alternatively, when the light-shielding film **10214** is formed, a display device with little light leakage at the time of black display can be obtained.

The color filter **10215** is not necessarily formed on the second substrate **10216**. When the color filter **10215** is not formed, the number of steps is reduced, so that manufacturing cost can be reduced. In addition, since a structure is simple when the color filter **10215** is not formed, yield can be improved. Note that even when the color filter **10215** is not formed, a display device which can perform color display can be obtained by field sequential driving. Alternatively, when the color filter **10215** is formed, a display device which can perform color display can be obtained.

Spherical spacers may be dispersed on the second substrate **10216** instead of forming the spacer **10217**. When the spherical spacers are dispersed, the number of steps is reduced, so that manufacturing cost can be reduced. In addition, since a structure is simple when the spherical spacers are dispersed, yield can be improved. Alternatively, when the spacer **10217** is formed, a distance between the two substrates can be uniform because a position of the spacer is not varied, so that a display device with little display unevenness can be obtained.

A process to be performed to the first substrate **10201** is described.

First, a first insulating film **10202** is formed over the first substrate **10201** by sputtering, a printing method, a coating method, or the like. Note that the first insulating film **10202** is not necessarily formed. The first insulating film **10202** has a function of preventing change in characteristics of the transistor due to an impurity from the first substrate **10201** which affects a semiconductor layer.

Next, a first conductive layer **10203** is formed over the first insulating film **10202** by photolithography, a laser direct writing method, an inkjet method, or the like.

Next, a second insulating film **10204** is formed over the entire surface by sputtering, a printing method, a coating method, or the like. The second insulating film **10204** has a function of preventing change in characteristics of the transistor due to an impurity from the first substrate **10201** which affects the semiconductor layer.

Next, a first semiconductor layer **10205** and a second semiconductor layer **10206** are formed. Note that the first semiconductor layer **10205** and the second semiconductor layer **10206** are formed sequentially and shapes thereof are processed at the same time.

Next, a second conductive layer **10207** is formed by photolithography, a laser direct writing method, an inkjet method, or the like. Note that as a method for etching which is performed at the time of processing a shape of the second conductive layer **10207**, dry etching is preferable. Note that as the second conductive layer **10207**, either a light-transmitting material or a reflective material may be used.

Next, a channel formation region of the transistor is formed. Here, an example of a step thereof is described. The second semiconductor layer **10206** is etched by using the second conductive layer **10207** as a mask. Alternatively, the second semiconductor layer **10206** is etched by using a mask for processing the shape of the second conductive layer **10207**. Then, the first conductive layer **10203** at a position where the second semiconductor layer **10206** is removed serves as the channel formation region of the transistor. Thus, the number of masks can be reduced, so that manufacturing cost can be reduced.

Next, a third insulating film **10208** is formed and a contact hole is selectively formed in the third insulating film **10208**. Note that a contact hole may be formed also in the second insulating film **10204** at the same time as forming the contact hole in the third insulating film **10208**.

Next, a third conductive layer **10209** is formed by photolithography, a laser direct writing method, an inkjet method, or the like.

Next, a first alignment film **10210** is formed. Note that after the first alignment film **10210** is formed, rubbing may be performed so as to control the alignment of the liquid crystal molecules. Rubbing is a step of forming stripes on an alignment film by rubbing the alignment film with a cloth. By performing rubbing, the alignment film can have alignment properties.

The first substrate **10201** which is manufactured as described above and the second substrate **10216** on which the light-shielding film **10214**, the color filter **10215**, the fourth conductive layer **10213**, the spacer **10217**, and the second alignment film **10212** are manufactured are attached to each other by a sealant with a gap of several μm therebetween. Then, a liquid crystal material is injected into a space between the two substrates. Note that in the MVA mode, the fourth conductive layer **10213** is formed over the entire surface of the second substrate **10216**. Note that the alignment control protrusion **10219** is formed so as to be in contact with the fourth conductive layer **10213**. The alignment control protrusion **10219** preferably has a shape with a smooth curved surface. Thus, alignment of the adjacent liquid crystal molecules **10218** is extremely similar, so that an alignment defect can be reduced. Further, a defect of the alignment film caused by breaking of the alignment film can be reduced.

FIG. **23**B is an example of a cross-sectional view of a pixel in the case where a PVA (patterned vertical alignment) mode and a transistor are combined. By applying the pixel structure shown in FIG. **23**B to a liquid crystal display device, a liquid crystal display device having a wide viewing angle, high response speed, and high contrast can be obtained.

Features of the pixel structure shown in FIG. **23**B are described. Liquid crystal molecules **10248** shown in FIG. **23**B are long and narrow molecules each having a major axis and a minor axis. In FIG. **23**B, direction of each of the liquid crystal molecules **10248** is expressed by the length thereof. That is, the direction of the major axis of the liquid crystal molecule **10248**, which is expressed as long, is parallel to the page, and as the liquid crystal molecule **10248** is expressed to be shorter, the direction of the major axis becomes closer to a normal direction of the page. That is, each of the liquid crystal molecules **10248** shown in FIG. **23**B is aligned such that the direction of the major axis is normal to the alignment film. Thus, the liquid crystal molecules **10248** at a position where an electrode notch portion **10249** is formed are aligned radially with a boundary of the electrode notch portion **10249** and the fourth conductive layer **10243** as a center. With this state, a liquid crystal display device having a wide viewing angle can be obtained.

Note that the case is described in which a bottom-gate transistor using an amorphous semiconductor is used as the transistor. In the case where a transistor using an amorphous semiconductor is used, a liquid crystal display device can be formed at low cost by using a large substrate.

A liquid crystal display device includes a basic portion displaying images, which is called a liquid crystal panel. The liquid crystal panel is manufactured as follows: two processed substrates are attached to each other with a gap of several μm therebetween, and a liquid crystal material is injected into a space between the two substrates. In FIG. **23**B, the two substrates correspond to the first substrate **10231** and the second substrate **10246**. A transistor and a pixel electrode are formed over the first substrate. A light-shielding film **10244**, a color filter **10245**, a fourth conductive layer **10243**, a spacer **10247**, and a second alignment film **10242** are formed on the second substrate.

The light-shielding film **10244** is not necessarily formed on the second substrate **10246**. When the light-shielding film **10244** is not formed, the number of steps is reduced, so that manufacturing cost can be reduced. In addition, since a structure is simple when the light-shielding film **10244** is not formed, yield can be improved. Alternatively, when the light-shielding film **10244** is formed, a display device with little light leakage at the time of black display can be obtained.

The color filter **10245** is not necessarily formed on the second substrate **10246**. When the color filter **10245** is not formed, the number of steps is reduced, so that manufacturing cost can be reduced. In addition, since a structure is simple when the color filter **10245** is not formed, yield can be improved. Note that even when the color filter **10245** is not formed, a display device which can perform color display can be obtained by field sequential driving. Alternatively, when the color filter **10245** is formed, a display device which can perform color display can be obtained.

Spherical spacers may be dispersed on the second substrate **10246** instead of forming the spacer **10247**. When the spherical spacers are dispersed, the number of steps is reduced, so that manufacturing cost can be reduced. In addition, since a structure is simple when the spherical spacers are dispersed, yield can be improved. Alternatively, when the spacer **10247** is formed, a distance between the two substrates can be uniform because a position of the spacer is not varied, so that a display device with little display unevenness can be obtained.

A process to be performed to the first substrate **10231** is described.

First, a first insulating film **10232** is formed over the first substrate **10231** by sputtering, a printing method, a coating method, or the like. Note that the first insulating film **10232** is not necessarily formed. The first insulating film **10232** has a function of preventing change in characteristics of the transistor due to an impurity from the first substrate **10231** which affects a semiconductor layer.

Next, a first conductive layer **10233** is formed over the first insulating film **10232** by photolithography, a laser direct writing method, an inkjet method, or the like.

Next, a second insulating film **10234** is formed over the entire surface by sputtering, a printing method, a coating method, or the like. The second insulating film **10234** has a function of preventing change in characteristics of the transistor due to an impurity from the first substrate **10231** which affects the semiconductor layer.

Next, a first semiconductor layer **10235** and a second semiconductor layer **10236** are formed. Note that the first semiconductor layer **10235** and the second semiconductor layer **10236** are formed sequentially and shapes thereof are processed at the same time.

Next, a second conductive layer **10237** is formed by photolithography, a laser direct writing method, an inkjet method, or the like. Note that as a method for etching which is performed at the time of processing a shape of the second conductive layer **10237**, dry etching is preferable. Note that as the second conductive layer **10237**, either a light-transmitting material or a reflective material may be used.

Next, a channel formation region of the transistor is formed. Here, an example of a step thereof is described. The second semiconductor layer **10236** is etched by using the second conductive layer **10237** as a mask. Alternatively, the second semiconductor layer **10236** is etched by using a mask for processing the shape of the second conductive layer **10107**. Then, the first conductive layer **10233** at a position where the second semiconductor layer **10236** is removed serves as the channel formation region of the transistor. Thus, the number of masks can be reduced, so that manufacturing cost can be reduced.

Next, a third insulating film **10238** is formed and a contact hole is selectively formed in the third insulating film **10238**. Note that a contact hole may be formed also in the second insulating film **10234** at the same time as forming the contact hole in the third insulating film **10238**. Note that a surface of the third insulating film **10238** is preferably as even as possible. This is because alignment of the liquid crystal molecules are affected by unevenness of a surface with which the liquid crystal is in contact.

Next, a third conductive layer **10239** is formed by photolithography, a laser direct writing method, an inkjet method, or the like.

Next, a first alignment film **10240** is formed. Note that after the first alignment film **10240** is formed, rubbing may be performed so as to control the alignment of the liquid crystal molecules. Rubbing is a step of forming stripes on an alignment film by rubbing the alignment film with a cloth. By performing rubbing, the alignment film can have alignment properties.

The first substrate **10231** which is manufactured as described above and the second substrate **10246** on which the light-shielding film **10244**, the color filter **10245**, the fourth conductive layer **10243**, the spacer **10247**, and the second alignment film **10242** are manufactured are attached to each other by a sealant with a gap of several μm therebetween. Then, a liquid crystal material is injected into a space between the two substrates. Note that in the PVA mode, the fourth conductive layer **10243** is patterned and is provided with the electrode notch portion **10249**. Although a shape of the electrode notch portion **10249** is not particularly limited, the electrode notch portion **10249** preferably has a shape in which a plurality of rectangles having different directions are combined. Thus, a plurality of regions having different alignment can be formed, so that a liquid crystal display device having a wide viewing angle can be obtained. Note that the fourth conductive layer **10243** at the boundary between the electrode notch portion **10249** and the fourth conductive layer **10243** preferably has a shape with a smooth curved surface. Thus, alignment of the adjacent liquid crystal molecules **10248** is extremely similar, so that an alignment defect is reduced. Further, a defect of the alignment film caused by breaking of the second alignment film **10242** by the electrode notch portion **10249** can be prevented.

FIG. **24**A is an example of a cross-sectional view of a pixel in the case where an IPS (in-plane-switching) mode and a transistor are combined. By applying the pixel structure shown in FIG. **24**A to a liquid crystal display device, a liquid crystal display device theoretically having a wide viewing angle and response speed which has low dependency on a gray scale can be obtained.

Features of the pixel structure shown in FIG. **24**A are described. Liquid crystal molecules **10318** shown in FIG. **24**A are long and narrow molecules each having a major axis and a minor axis. In FIG. **24**A, a direction of each of the liquid crystal molecules **10318** is expressed by the length thereof. That is, the direction of the major axis of the liquid crystal molecule **10318**, which is expressed as long, is parallel to the page, and as the liquid crystal molecule **10318** is expressed to be shorter, the direction of the major axis becomes closer to a normal direction of the page. That is, each of the liquid crystal molecules **10318** shown in FIG. **24**A is aligned so that the direction of the major axis thereof is always horizontal to the substrate. Although FIG. **24**A shows alignment with no electric field, when an electric field is applied to each of the liquid crystal molecules **10318**, each of the liquid crystal molecules **10318** rotates in a horizontal plane as the direction of the major axis thereof is always horizontal to the substrate. With this state, a liquid crystal display device having a wide viewing angle can be obtained.

Note that the case is described in which a bottom-gate transistor using an amorphous semiconductor is used as the transistor. In the case where a transistor using an amorphous semiconductor is used, a liquid crystal display device can be formed at low cost by using a large substrate.

A liquid crystal display device includes a basic portion displaying images, which is called a liquid crystal panel. The liquid crystal panel is manufactured as follows: two processed substrates are attached to each other with a gap of several μm therebetween, and a liquid crystal material is injected into a space between the two substrates. In FIG. **24**A, the two substrates correspond to the first substrate **10301** and the second substrate **10316**. A transistor and a pixel electrode are formed over the first substrate. A light-shielding film **10314**, a color filter **10315**, a fourth conductive layer **10313**, a spacer **10317**, and a second alignment film **10312** are formed on the second substrate.

The light-shielding film **10314** is not necessarily formed on the second substrate **10316**. When the light-shielding film **10314** is not formed, the number of steps is reduced, so that manufacturing cost can be reduced. In addition, since a structure is simple when the light-shielding film **10314** is not formed, yield can be improved. Alternatively, when the light-shielding film **10314** is formed, a display device with little light leakage at the time of black display can be obtained.

The color filter **10315** is not necessarily formed on the second substrate **10316**. When the color filter **10315** is not formed, the number of steps is reduced, so that manufacturing cost can be reduced. In addition, since a structure is simple when the color filter **10315** is not formed, yield can be improved. Note that even when the color filter **10315** is not formed, a display device which can perform color display can be obtained by field sequential driving. Alternatively, when the color filter **10315** is formed, a display device which ran perform color display can be obtained.

Spherical spacers may be dispersed on the second substrate **10316** instead of forming the spacer **10317**. When the spherical spacers are dispersed, the number of steps is reduced, so that manufacturing cost can be reduced. In addition, since a structure is simple when the spherical spacers are dispersed, yield can be improved. Alternatively, when the spacer **10317** is formed, a distance between the two substrates can be uniform because a position of the spacer is not varied, so that a display device with little display unevenness can be obtained.

A process to be performed to the first substrate **10301** is described.

First, a first insulating film **10302** is formed over the first substrate **10301** by sputtering, a printing method, a coating method, or the like. Note that the first insulating film **10302** is not necessarily formed. The first insulating film **10302** has a function of preventing change in characteristics of the transistor due to an impurity from the first substrate **10301** which affects a semiconductor layer.

Next, a first conductive layer **10303** is formed over the first insulating film **10302** by photolithography, a laser direct writing method, an inkjet method, or the like.

Next, a second insulating film **10304** is formed over the entire surface by sputtering, a printing method, a coating method, or the like. The second insulating film **10304** has a function of preventing change in characteristics of the transistor due to an impurity from the first substrate **10301** which affects the semiconductor layer.

Next, a first semiconductor layer **10305** and a second semiconductor layer **10306** are formed. Note that the first semiconductor layer **10305** and the second semiconductor layer **10306** are formed sequentially and shapes thereof are processed at the same time.

Next, a second conductive layer **10307** is formed by photolithography, a laser direct writing method, an inkjet method, or the like. Note that as a method for etching which is performed at the time of processing a shape of the second conductive layer **10307**, dry etching is preferable. Note that as the second conductive layer **10307**, either a light-transmitting material or a reflective material may be used.

Next, a channel formation region of the transistor is formed. Here, an example of a step thereof is described. The second semiconductor layer **10106** is etched by using the second conductive layer **10307** as a mask. Alternatively, the second semiconductor layer **10306** is etched by using a mask for processing the shape of the second conductive layer **10307**. Then, the first conductive layer **10303** at a position where the second semiconductor layer **10306** is removed serves as the channel formation region of the transistor. Thus, the number of masks can be reduced, so that manufacturing cost can be reduced.

Next, a third insulating film **10308** is formed and a contact hole is selectively formed in the third insulating film **10308**. Note that a contact hole may be formed also in the second insulating film **10304** at the same time as forming the contact hole in the third insulating film **10308**.

Next, a third conductive layer **10309** is formed by photolithography, a laser direct writing method, an inkjet method, or the like. Here, the third conductive layer **10309** has a shape in which two comb-shaped electrodes engage with each other. One of the comb-shaped electrodes is electrically connected to one of a source electrode and a drain electrode of the transistor, and the other of the comb-shaped electrodes is electrically connected to a common electrode. Thus, a horizontal electric field can be effectively applied to the liquid crystal molecules **10318**.

Next, a first alignment film **10310** is formed. Note that after the first alignment film **10310** is formed, rubbing may be performed so as to control the alignment of the liquid crystal molecules. Rubbing is a step of forming stripes on an alignment film by rubbing the alignment film with a cloth. By performing rubbing, the alignment film can have alignment properties.

The first substrate **10301** which is manufactured as described above and the second substrate **10316** on which the light-shielding film **10314**, the color filter **10315**, the spacer **10317**, and the second alignment film **10312** are formed are attached to each other by a sealant with a gap of several μm therebetween. Then, a liquid crystal material is injected into a space between the two substrates.

FIG. **24**B is an example of a cross-sectional view of a pixel in the case where an FFS (fringe field switching) mode and a transistor are combined. By applying the pixel structure shown in FIG. **24**B to a liquid crystal display device, a liquid crystal display device theoretically having a wide viewing angle and response speed which has low dependency on a gray scale can be obtained.

Features of the pixel structure shown in FIG. **24**B are described. Liquid crystal molecules **10348** shown in FIG. **24**B are long and narrow molecules each having a major axis and a minor axis. In FIG. **24**B, direction of each of the liquid crystal molecules **10348** is expressed by the length thereof. That is, the direction of the major axis of the liquid crystal molecule **10348**, which is expressed as long, is parallel to the page, and as the liquid crystal molecule **10348** is expressed to be shorter, the direction of the major axis becomes closer to a normal direction of the page. That is, each of the liquid crystal molecules **10348** shown in FIG. **24**B is aligned so that the direction of the major axis thereof is always horizontal to the substrate. Although FIG. **24**B shows alignment with no electric field, when an electric field is applied to each of the liquid crystal molecules **10348**, each of the liquid crystal molecules **10348** rotates in a horizontal plane as the direction of the major axis thereof is always horizontal to the substrate. With this state, a liquid crystal display device having a wide viewing angle can be obtained.

Note that the case is described in which a bottom-gate transistor using an amorphous semiconductor is used as the transistor. In the case where a transistor using an amorphous semiconductor is used, a liquid crystal display device can be formed at low cost by using a large substrate.

A liquid crystal display device includes a basic portion displaying images, which is called a liquid crystal panel. The liquid crystal panel is manufactured as follows: two processed substrates are attached to each other with a gap of several μm therebetween, and a liquid crystal material is injected into a space between the two substrates. In FIG. **24**B, the two substrates correspond to the first substrate **10331** and the second substrate **10346**. A transistor and a pixel electrode are formed over the first substrate. A light-shielding film **10344**, a color filter **10345**, a fourth conductive layer **10343**, a spacer **10347**, and a second alignment film **10342** are formed on the second substrate.

The light-shielding film **10344** is not necessarily formed on the second substrate **10346**. When the light-shielding film **10344** is not formed, the number of steps is reduced, so that manufacturing cost can be reduced. In addition, since a structure is simple when the light-shielding film **10344** is not formed, yield can be improved. Alternatively, when the light-shielding film **10344** is formed, a display device with little light leakage at the time of black display can be obtained.

The color filter **10345** is not necessarily formed on the second substrate **10346**. When the color filter **10345** is not formed, the number of steps is reduced, so that manufacturing cost can be reduced. In addition, since a structure is simple when the color filter **10345** is not formed, yield can be improved. Note that even when the color filter **10345** is not formed, a display device which can perform color display can be obtained by field sequential driving. Alternatively, when the color filter **10345** is formed, a display device which can perform color display can be obtained.

Spherical spacers may be dispersed on the second substrate **10346** instead of forming the spacer **10347**. When the spherical spacers are dispersed, the number of steps is reduced, so that manufacturing cost can be reduced. In addition, since a structure is simple when the spherical spacers are dispersed, yield can be improved. Alternatively, when the spacer **10347** is formed, a distance between the two substrates can be uniform because a position of the spacer is not varied, so that a display device with little display unevenness can be obtained.

A process to be performed to the first substrate **10331** is described.

First, a first insulating film **10332** is formed over the first substrate **10331** by sputtering, a printing method, a coating method, or the like. Note that the first insulating film **10332** is not necessarily formed. The first insulating film **10332** has a function of preventing change in characteristics of the transistor due to an impurity from the first substrate **10331** which affects a semiconductor layer.

Next, a first conductive layer **10333** is formed over the first insulating film **10332** by photolithography, a laser direct writing method, an inkjet method, or the like.

Next, a second insulating film **10334** is formed over the entire surface by sputtering, a printing method, a coating method, or the like. The second insulating film **10334** has a function of preventing change in characteristics of the transistor due to an impurity from the first substrate **10331** which affects the semiconductor layer.

Next, a first semiconductor layer **10335** and a second semiconductor layer **10336** are formed. Note that the first semiconductor layer **10335** and the second semiconductor layer **10336** are formed sequentially and shapes thereof are processed at the same time.

Next, a second conductive layer **10337** is formed by photolithography, a laser direct writing method, an inkjet method, or the like. Note that as a method for etching which is performed at the time of processing a shape of the second conductive layer **10337**, dry etching is preferable. Note that as the second conductive layer **10337**, either a light-transmitting material or a reflective material may be used.

Next, a channel formation region of the transistor is formed. Here, an example of a step thereof is described. The second semiconductor layer **10106** is etched by using the second conductive layer **10337** as a mask. Alternatively, the second semiconductor layer **10336** is etched by using a mask for processing the shape of the second conductive layer **10337**. Then, the first conductive layer **10333** at a position where the second semiconductor layer **10336** is removed serves as the channel formation region of the transistor. Thus, the number of masks can be reduced, so that manufacturing cost can be reduced.

Next, a third insulating film **10338** is formed and a contact hole is selectively formed in the third insulating film **10338**.

Next, a fourth conductive layer **10343** is formed by photolithography, a laser direct writing method, an inkjet method, or the like.

Next, a fourth insulating film **10349** is formed and a contact hole is selectively formed in the fourth insulating film **10349**. Note that a surface of the fourth insulating film **10349** is preferably as even as possible. This is because alignment of the liquid crystal molecules are affected by unevenness of a surface with which the liquid crystal is in contact.

Next, a third conductive layer **10339** is formed by photolithography, a laser direct writing method, an inkjet method, or the like. Here, the third conductive layer **10339** is comb-shaped.

Next, a first alignment film **10340** is formed. Note that after the first alignment film **10340** is formed, rubbing may be performed so as to control the alignment of the liquid crystal molecules. Rubbing is a step of forming stripes on an alignment film by rubbing the alignment film with a cloth. By performing rubbing, the alignment film can have alignment properties.

The first substrate **10331** which is manufactured as described above and the second substrate **10346** on which the light-shielding film **10344**, the color filter **10345**, the spacer **10347**, and the second alignment film **10342** are formed are attached to each other by a sealant with a gap of several μm therebetween. Then, a liquid crystal material is injected into a space between the two substrates. Therefore, a liquid crystal panel can be manufactured.

Here, materials which can be used for conductive layers or insulating films are described.

As the first insulating film **10102** in FIG. **22**, the first insulating film **10202** in FIG. **23**A, the first insulating film **10232** in FIG. **23**B, the first insulating film **10302** in FIG. **24**A, or the first insulating film **10332** in FIG. **24**B, an insulating film such as a silicon oxide film, a silicon nitride film, or a silicon oxynitride (SiO_xN_y) film can be used. Alternatively, an insulating film having a stacked-layer structure in which two or more of a silicon oxide film, a silicon nitride film, a silicon oxynitride (SiO_xN_y) film, and the like are combined can be used as.

As the first conductive layer **10103** in FIG. **22**, the first conductive layer **10203** in FIG. **23**A, the first conductive layer **10233** in FIG. **23**B, the first conductive layer **10303** in FIG. **24**A, or the first conductive layer **10333** in FIG. **24**B, Mo, Ti, Al, Nd, Cr, or the like can be used. Alternatively, a stacked-layer structure in which two or more of Mo, Ti, Al, Nd, Cr, and the like are combined can be used.

As the second insulating film **10104** in FIG. **22**, the second insulating film **10204** in FIG. **23**A, the second insulating film **10234** in FIG. **23**B, the second insulating film **10304** in FIG. **24**A, or the second insulating film **10334** in FIG. **24**B, a thermal oxide film, a silicon oxide film, a silicon nitride film, a silicon oxynitride film, or the like can be used. Alternatively, a stacked-layer structure in which two or more of a thermal oxide film, a silicon oxide film, a silicon nitride film, a silicon oxynitride film, and the like are combined can be used. Note that a silicon oxide film is preferable in a portion which is in contact with a semiconductor layer. This is because a trap level at an interface with the semiconductor layer decreases when a silicon oxide film is used. Note that a silicon nitride film is preferable in a portion which is in contact with Mo. This is because a silicon nitride film does not oxidize Mo.

As the first semiconductor layer **10105** in FIG. **22**, the first semiconductor layer **10205** in FIG. **23**A, the first semiconductor layer **10235** in FIG. **23**B, the first semiconductor layer **10305** in FIG. **24**A, or the first semiconductor layer **10335** in FIG. **24**B, silicon, silicon germanium (SiGe), or the like can be used.

As the second semiconductor layer **10106** in FIG. **22**, the second semiconductor layer **10206** in FIG. **23**A, the second semiconductor layer **10236** in FIG. **23**B, the second semiconductor layer **10306** in FIG. **24**A, or the second semiconductor layer **10336** in FIG. **24**B, silicon or the like including phosphorus can be used, for example.

As a light-transmitting material of the second conductive layer **10107** and the third conductive layer **10109** in FIG. **22**; the second conductive layer **10207** and the third conductive layer **10209** in FIG. **23**A; the second conductive layer **10237** and the third conductive layer **10239** in FIG. **23**B; the second conductive layer **10307** and the third conductive layer **10309** in FIG. **24**A; or the second conductive layer **10337**, the third conductive layer **10339**, and a fourth conductive layer **10343** in FIG. **24**B, an indium tin oxide (ITO) film formed by mixing tin oxide into indium oxide, an indium tin silicon oxide (ITSO) film formed by mixing silicon oxide into indium tin oxide (ITO), an indium zinc oxide (IZO) film formed by mixing zinc oxide into indium oxide, a zinc oxide film, a tin oxide film, or the like can be used. Note that IZO is a light-transmitting conductive material formed by sputtering using a target in which zinc oxide (ZnO) is mixed into ITO at 2 to 20 wt %.

As a reflective material of the second conductive layer **10107** and the third conductive layer **10109** in FIG. **22**; the second conductive layer **10207** and the third conductive layer **10209** in FIG. **23**A; the second conductive layer **10237** and the third conductive layer **10239** in FIG. **23**B; the second conductive layer **10307** and the third conductive layer **10309** in FIG. **24**A; or the second conductive layer **10337**, the third conductive layer **10339**, and the fourth conductive layer **10343** in FIG. **24**B, Ti, Mo, Ta, Cr, W, Al, or the like can be used. Alternatively, a two-layer structure in which Al and Ti, Mo, Ta, Cr, or W are stacked, or a three-layer structure in which Al is interposed between metals such as Ti, Mo, Ta, Cr, and W may be used.

As the third insulating film **10108** in FIG. **22**, the third insulating film **10208** in FIG. **23**A, the third insulating film **10238** in FIG. **23**B, the third conductive layer **10239** in FIG. **23**B, the third insulating film **10308** in FIG. **24**A, or the third insulating film **10338** and the fourth insulating film **10349** in FIG. **24**B, an inorganic material (e.g., silicon oxide, silicon nitride, or silicon oxynitride), an organic compound material having a low dielectric constant (e.g., a photosensitive or nonphotosensitive organic resin material), or the like can be used. Alternatively, a material including siloxane can be used. Note that siloxane is a material in which a skeleton structure is formed by a bond of silicon (Si) and oxygen (O). As a substituent, an organic group including at least hydrogen (e.g., an alkyl group or aromatic hydrocarbon) is used. Alternatively, a fluoro group may be used as the substituent. Further alternatively, the organic group including at least hydrogen and the fluoro group may be used as the substituent.

As the first alignment film **10110** in FIG. **22**, the first alignment film **10210** in FIG. **23**A, the first alignment film **10240** in FIG. **2313**, the first alignment film **10310** in FIG. **24**A, or the first alignment film **10340** in FIG. **24**B, a film of a high molecular compound such as polyimide can be used.

Next, the pixel structure in the case where each liquid crystal mode and the transistor are combined is described with reference to a top plan view (a layout diagram) of the pixel.

Note that as a liquid crystal mode, a TN (twisted nematic) mode, an IPS (in-plane-switching) mode, an FFS (fringe field switching) mode, an MVA (multi-domain vertical alignment) mode, a PVA (patterned vertical alignment) mode, an ASM (axially symmetric aligned micro-cell) mode, an OCB (optical compensated birefringence) mode, an FLC (ferroelectric liquid crystal) mode, an AFLC (antiferroelectric liquid crystal) mode, or the like can be used.

As the transistor, a thin film transistor (a TFT) including a non-single crystalline semiconductor layer typified by amorphous silicon, polycrystalline silicon, microcrystalline (also referred to as semi-amorphous) silicon, or the like can be used.

Note that as a structure of the transistor, a top-gate structure, a bottom-gate structure, or the like can be used. A channel-etched transistor, a channel-protective transistor, or the like can be used as a bottom-gate transistor.

FIG. **25** is an example of a top plan view of a pixel in the case where a TN mode and a transistor are combined. By applying the pixel structure shown in FIG. **25** to a liquid crystal display device, a liquid crystal display device can be formed at low cost.

The pixel shown in FIG. **25** includes a scan line **10401**, an image signal line **10402**, a capacitor line **10403**, a transistor **10404**, a pixel electrode **10405**, and a pixel capacitor **10406**.

The scan line **10401** has a function of transmitting a signal (a scan signal) to the pixel. The image signal line **10402** has a function for transmitting a signal (an image signal) to the pixel. Note that since the scan line **10401** and the image signal line **10402** are arranged in matrix, they are formed of conductive layers in different layers. Note that a semiconductor layer may be provided at an intersection of the scan line **10401** and the image signal line **10402**. Thus, intersection capacitance formed between the scan line **10401** and the image signal line **10402** can be reduced.

The capacitor line **10403** is provided in parallel to the pixel electrode **10405**. A portion where the capacitor line **10403** and the pixel electrode **10405** overlap with each other corresponds to the pixel capacitor **10406**. Note that part of the capacitor line **10403** is extended along the image signal line **10402** so as to surround the image signal line **10402**. Thus, crosstalk can be reduced. Crosstalk is a phenomenon in which a potential of an electrode, which should hold the potential, is changed in accordance with change in potential of the image signal line **10402**. Note that intersection capacitance can be reduced by providing a semiconductor layer between the capacitor line **10403** and the image signal line **10402**. Note that the capacitor line **10403** is formed of a material which is similar to that of the scan line **10401**.

The transistor **10404** has a function as a switch which turns on the image signal line **10402** and the pixel electrode **10405**.

Note that one of a source region and a drain region of the transistor **10404** is provided so as to be surrounded by the other of the source region and the drain region of the transistor **10404**. Thus, the channel width of the transistor **10404** increases, so that switching capability can be improved. Note that a gate electrode of the transistor **10404** is provided so as to surround the semiconductor layer.

The pixel electrode **10405** is electrically connected to one of a source electrode and a drain electrode of the transistor **10404**. The pixel electrode **10405** is an electrode for applying signal voltage which is transmitted by the image signal line **10402** to a liquid crystal element. Note that the pixel electrode **10405** is rectangular. Thus, an aperture ratio can be improved. Note that as the pixel electrode **10405**, a light-transmitting material or a reflective material may be used. Alternatively, the pixel electrode **10405** may be formed by combining a light-transmitting material and a reflective material.

FIG. **26**A is an example of a top plan view of a pixel in the case where an MVA mode and a transistor are combined. By applying the pixel structure shown in FIG. **26**A to a liquid crystal display device, a liquid crystal display device having a wide viewing angle, high response speed, and high contrast can be obtained.

The pixel shown in FIG. **26**A includes a scan line **10501**, a video signal line **10502**, a capacitor line **10503**, a transistor **10504**, a pixel electrode **10505**, a pixel capacitor **10506**, and an alignment control protrusion **10507**.

The scan line **10501** has a function of transmitting a signal (a scan signal) to the pixel. The image signal line **10502** has a function for transmitting a signal (an image signal) to the pixel. Note that since the scan line **10501** and the image signal line **10502** are arranged in matrix, they are formed of conductive layers in different layers. Note that a semiconductor layer may be provided at an intersection of the scan line **10501** and the image signal line **10502**. Thus, intersection capacitance formed between the scan line **10501** and the image signal line **10502** can be reduced.

The capacitor line **10503** is provided in parallel to the pixel electrode **10505**. A portion where the capacitor line **10503** and the pixel electrode **10505** overlap with each other corresponds to the pixel capacitor **10506**. Note that part of the capacitor line **10503** is extended along the image signal line **10502** so as to surround the image signal line **10502**. Thus, crosstalk can be reduced. Crosstalk is a phenomenon in which a potential of an electrode, which should hold the potential, is changed in accordance with change in potential of the image signal line **10502**. Note that intersection capacitance can be reduced by providing a semiconductor layer between the capacitor line **10503** and the image signal line **10502**. Note that the capacitor line **10503** is formed of a material which is similar to that of the scan line **10501**.

The transistor **10504** has a function as a switch which turns on the image signal line **10502** and the pixel electrode **10505**. Note that one of a source region and a drain region of the transistor **10504** is provided so as to be surrounded by the other of the source region and the drain region of the transistor **10504**. Thus, the channel width of the transistor **10504** increases, so that switching capability can be improved. Note that a gate electrode of the transistor **10504** is provided so as to surround the semiconductor layer.

The pixel electrode **10505** is electrically connected to one of a source electrode and a drain electrode of the transistor **10504**. The pixel electrode **10505** is an electrode for applying signal voltage which is transmitted by the image signal line **10502** to a liquid crystal element. Note that the pixel electrode **10505** is rectangular. Thus, an aperture ratio can be improved. Note that as the pixel electrode **10505**, a light-transmitting material or a reflective material may be used. Alternatively, the pixel electrode **10505** may be formed by combining a light-transmitting material and a reflective material.

The alignment control protrusion **10507** is formed on a counter substrate. The alignment control protrusion **10507** has a function of aligning liquid crystal molecules radially. Note that a shape of the alignment control protrusion **10507** is not particularly limited. For example, the alignment control protrusion **10507** may be a dogleg shape. Thus, a plurality of regions having different alignment of the liquid crystal molecules can be formed, so that a viewing angle can be improved.

FIG. **26**B is an example of a top plan view of a pixel in the case where a PVA mode and a transistor are combined. By applying the pixel structure shown in FIG. **26**B to a liquid crystal display device, a liquid crystal display device having a wide viewing angle, high response speed, and high contrast can be obtained.

The pixel shown in FIG. **26**B includes a scan line **10511**, a video signal line **10512**, a capacitor line **10513**, a transistor **10514**, a pixel electrode **10515**, a pixel capacitor **10516**, and an electrode notch portion **10517**.

The scan line **10511** has a function of transmitting a signal (a scan signal) to the pixel. The image signal line **10512** has a function for transmitting a signal (an image signal) to the pixel. Note that since the scan line **10511** and the image signal line **10512** are arranged in matrix, they are formed of conductive layers in different layers. Note that a semiconductor layer may be provided at an intersection of the scan line **10511** and the image signal line **10512**. Thus, intersection capacitance formed between the scan line **10511** and the image signal line **10512** can be reduced.

The capacitor line **10513** is provided in parallel to the pixel electrode **10515**. A portion where the capacitor line **10513** and the pixel electrode overlap with each other corresponds to the pixel capacitor **10516**. Note that part of the capacitor line **10513** is extended along the image signal line **10512** so as to surround the image signal line **10512**. Thus; crosstalk can be reduced. Crosstalk is a phenomenon in which a potential of an electrode, which should hold the potential, is changed in accordance with change in potential of the image signal line **10512**. Note that intersection capacitance can be reduced by providing a semiconductor layer between the capacitor line **10513** and the image signal line **10512**. Note that the capacitor line **10513** is formed of a material which is similar to that of the scan line **10511**.

The transistor **10514** has a function as a switch which turns on the image signal line **10512** and the pixel electrode **10515**. Note that one of a source region and a drain region of the transistor **10514** is provided so as to be surrounded by the other of the source region and the drain region of the transistor **10514**. Thus, the channel width of the transistor **10514** increases, so that switching capability can be improved. Note that a gate electrode of the transistor **10514** is provided so as to surround the semiconductor layer.

The pixel electrode **10515** is electrically connected to one of a source electrode and a drain electrode of the transistor **10514**. The pixel electrode **10515** is an electrode for applying signal voltage which is transmitted by the image signal line **10512** to a liquid crystal element. Note that the pixel electrode **10515** has a shape which is formed in accordance with a shape of the electrode notch portion **10517**. Specifically, the pixel electrode **10515** has a shape in which a portion where the pixel electrode **10515** is notched is formed in a portion where the electrode notch portion **10517** is not formed. Thus, a plurality of regions having different alignment of the liquid crystal molecules can be formed, so that a viewing angle can be improved. Note that as the pixel electrode **10515**, a light-transmitting material or a reflective material may be used. Alternatively, the pixel electrode **10515** may be formed by combining a light-transmitting material and a reflective material.

FIG. **27**A is an example of a top plan view of a pixel in the case where an IPS mode and a transistor are combined. By applying the pixel structure shown in FIG. **27**A to a liquid crystal display device, a liquid crystal display device theoretically having a wide viewing angle and response speed which has low dependency on a gray scale can be obtained.

The pixel shown in FIG. **27**A includes a scan line **10601**, a video signal line **10602**, a common electrode **10603**, a transistor **10604**, and a pixel electrode **10605**.

The scan line **10601** has a function of transmitting a signal (a scan signal) to the pixel. The image signal line **10602** has a function of transmitting a signal (an image signal) to the pixel. Note that since the scan line **10601** and the image signal line **10602** are arranged in matrix, they are formed of conductive layers in different layers. Note that a semiconductor layer may be provided at an intersection of the scan line **10601** and the image signal line **10602**. Thus, intersection capacitance formed between the scan line **10601** and the image signal line **10602** can be reduced. Note that the image signal line **10602** is formed in accordance with a shape of the pixel electrode **10605**.

The common electrode **10603** is provided in parallel to the pixel electrode **10605**. The common electrode **10603** is an electrode for generating a horizontal electric field. Note that the common electrode **10603** is bent comb-shaped. Note that part of the common electrode **10603** is extended along the image signal line **10602** so as to surround the image signal line **10602**. Thus, crosstalk can be reduced. Crosstalk is a phenomenon in which a potential of an electrode, which should hold the potential, is changed in accordance with change in potential of the image signal line **10602**. Note that intersection capacitance can be reduced by providing a semiconductor layer between the common electrode **10603** and the image signal line **10602**. Par of the common electrode **10603**, which is provided in parallel to the scan line **10601**, is formed of a material which is similar to that of the scan line **10601**. Part of the common electrode **10603**, which is provided in parallel to the pixel electrode **10605**, is formed of a material which is similar to that of the pixel electrode **10605**.

The transistor **10604** has a function as a switch which turns on the image signal line **10602** and the pixel electrode **10605**. Note that one of a source region and a drain region of the transistor **10604** is provided so as to be surrounded by the other of the source region and the drain region of the transistor **10604**. Thus, the channel width of the transistor **10604** increases, so that switching capability can be improved. Note that a gate electrode of the transistor **10604** is provided so as to surround the semiconductor layer.

The pixel electrode **10605** is electrically connected to one of a source electrode and a drain electrode of the transistor **10604**. The pixel electrode **10605** is an electrode for applying signal voltage which is transmitted by the image signal line **10602** to a liquid crystal element. Note that the pixel electrode **10605** is bent comb-shaped. Thus, a horizontal electric field can be applied to liquid crystal molecules. In addition, since a plurality of regions having different alignment of the liquid crystal molecules can be formed, a viewing angle can be improved. Note that as the pixel electrode **10605**, a light-transmitting material or a reflective material may be used. Alternatively, the pixel electrode **10605** may be formed by combining a light-transmitting material and a reflective material.

Note that a comb-shaped portion in the common electrode **10603** and the pixel electrode **10605** may be formed of different conductive layers. For example, the comb-shaped portion in the common electrode **10603** may be formed of a conductive layer which is the same as that of the scan line **10601** or the image signal line **10602**. Similarly, the pixel electrode **10605** may be formed of a conductive layer which is the same as that of the scan line **10601** or the image signal line **10602**.

FIG. **27**B is a top plan view of a pixel in the case where an FFS mode and a transistor are combined. By applying the pixel structure shown in FIG. **27**B to a liquid crystal display device, a liquid crystal display device theoretically having a wide viewing angle and response speed which has low dependency on a gray scale can be obtained.

The pixel shown in FIG. **27**B may include a scan line **10611**, a video signal line **10612**, a common electrode **10613**, a transistor **10614**, and a pixel electrode **10615**.

The scan line **10611** has a function of transmitting a signal (a scan signal) to the pixel. The image signal line **10612** has a function of transmitting a signal (an image signal) to the pixel. Note that since the scan line **10611** and the image signal line **10612** are arranged in matrix, they are formed of conductive layers in different layers. Note that a semiconductor layer may be provided at an intersection of the scan line **10611** and the image signal line **10612**. Thus, intersection capacitance formed between the scan line **10611** and the image signal line **10612** can be reduced. Note that the image signal line **10612** is formed in accordance with a shape of the pixel electrode **10615**.

The common electrode **10613** is formed uniformly below the pixel electrode **10615** and below and between the pixel electrodes **10615**. Note that as the common electrode **10613**, either a light-transmitting material or a reflective material may be used. Alternatively, the common electrode **10613** may be formed by combining a material in which a light-transmitting material and a reflective material.

The transistor **10614** has a function as a switch which turns on the image signal line **10612** and the pixel electrode **10615**. Note that one of a source region and a drain region of the transistor **10614** is provided so as to be surrounded by the other of the source region and the drain region of the transistor **10614**. Thus, the channel width of the transistor **10614** increases, so that switching capability can be improved. Note that a gate electrode of the transistor **10614** is provided so as to surround the semiconductor layer.

The pixel electrode **10615** is electrically connected to one of a source electrode and a drain electrode of the transistor **10614**. The pixel electrode **10615** is an electrode for applying signal voltage which is transmitted by the image signal line **10612** to a liquid crystal element. Note that the pixel electrode **10615** is bent comb-shaped. The comb-shaped pixel electrode **10615** is provided to be closer to a liquid crystal layer than a uniform portion of the common electrode **10613**. Thus, a horizontal electric field can be applied to liquid crystal molecules. In addition, a plurality of regions having different alignment of the liquid crystal molecules can be formed, so that a viewing angle can be improved. Note that as the pixel electrode **10615**, a light-transmitting material or a reflective material may be used. Alternatively, the pixel electrode **10615** may be formed by combining a light-transmitting material and a reflective material.

Note that although this embodiment mode is described with reference to various drawings, the contents (or may be part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in another drawing.

Further, even more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or may be part of the contents) described in each drawing of this embodiment mode can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in a drawing in another embodiment mode or embodiment. Further, even more drawings can be formed by combining each part with part of another embodiment mode or embodiment in the drawings of this embodiment mode.

This embodiment mode shows an example of an embodied case of the contents (or may be part of the contents) described in other embodiment modes and embodiments, an example of slight transformation thereof, an example of partial modification thereof, an example of improvement thereof, an example of detailed description thereof, an application example thereof, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment mode.

[Embodiment Mode 6]

In this embodiment mode, a peripheral portion of a liquid crystal panel is described.

FIG. **28** shows an example of a liquid crystal display device including a so-called edge-light type backlight unit **20101** and a liquid crystal panel **20107**. An edge-light type corresponds to a type in which a light source is provided at an end of a backlight unit and fluorescence of the light source is emitted from the entire light-emitting surface. The edge-light type backlight unit is thin and can save power.

The backlight unit **20101** includes a diffusion plate **20102**, a light guide plate **20103**, a reflection plate **20104**, a lamp reflector **20105**, and a light source **20106**.

The light source **20106** has a function of emitting light as necessary. For example, as the light source **20106**, a cold cathode fluorescent lamp, a hot cathode fluorescent lamp, a light-emitting diode, an inorganic EL element, an organic EL element, or the like is used. The lamp reflector **20105** has a function of efficiently guiding fluorescence from the light source **20106** to the light guide plate **20103**. The light guide plate **20103** has a function of guiding light to the entire surface by total reflection of fluorescence. The diffusion plate **20102** has a function of reducing variations in brightness. The reflection plate **20104** has a function of reflecting light which is leaked from the light guide plate **20103** downward (a direction which is opposite to the liquid crystal panel **20107**) to be reused.

Note that a control circuit for controlling luminance of the light source **20106** is connected to the backlight unit **20101**. By using this control circuit, luminance of the light source **20106** can be controlled.

FIGS. **29**A to **29**D are views each showing a detailed structure of the edge-light type backlight unit. Note that description of a diffusion plate, a light guide plate, a reflection plate, and the like is omitted.

A backlight unit **20201** shown in FIG. **29**A has a structure in which a cold cathode fluorescent lamp **20203** is used as a light source. In addition, a lamp reflector **20202** is provided to efficiently reflect light from the cold cathode fluorescent lamp **20203**. Such a structure is often used for a large display device because luminance of light obtained from the cold cathode fluorescent lamp is high.

A backlight unit **20211** shown in FIG. **2913** has a structure in which light-emitting diodes (LEDs) **20213** are used as light sources. For example, the light-emitting diodes (LEDs) **20213** which emit white light are provided at a predetermined interval. In addition, a lamp reflector **20212** is provided to efficiently reflect light from the light-emitting diodes (LEDs) **20213**.

Since luminance of light-emitting diodes is high, a structure using light-emitting diodes is suitable for a large display device. Since light-emitting diodes are superior in color reproductivity, an arrangement area can be reduced. Therefore, a frame of a display device can be narrowed.

Note that in the case where light-emitting diodes are mounted an a large display device, the light-emitting diodes can be provided on a back side of the substrate. The light-emitting diodes of R, G, and B are sequentially provided at a predetermined interval. By providing the light-emitting diodes, color reproductivity can be improved.

A backlight unit **20221** shown in FIG. **44**C has a structure in which light-emitting diodes (LEDs) **20223**, light-emitting diodes (LEDs) **20224**, and light-emitting diodes (LEDs) **20225** of R, G, and B are used as light sources. The light-emitting diodes (LEDs) **20223**, the light-emitting diodes (LEDs) **20224**, and the light-emitting diodes (LEDs) **20225** of R, G, and B are each provided at a predetermined interval. By using the light-emitting diodes (LEDs) **20223**, the light-emitting diodes (LEDs) **20224**, and the light-emitting diodes (LEDs) **20225** of R, G, and B, color reproductivity can be improved. In addition, a lamp reflector **20222** is provided to efficiently reflect light from the light-emitting diodes.

Since luminance of light-emitting diodes is high, a structure using light-emitting diodes is suitable for a large display device. Since light-emitting diodes are superior in color reproductivity, an arrangement area can be reduced. Therefore, a frame of a display device can be narrowed.

By sequentially making the light-emitting diodes of R, G, and B emit light in accordance with time, color display can be performed. This is a so-called field sequential mode.

Note that a light-emitting diode which emits white light can be combined with the light-emitting diodes (LEDs) **20223**, the light-emitting diodes (LEDs) **20224**, and the light-emitting diodes (LEDs) **20225** of R, G, and B.

Note that in the case where light-emitting diodes are mounted on a large display device, the light-emitting diodes can be provided on a back side of the substrate. The light-emitting diodes of R, G, and B are sequentially provided at a predetermined interval. By providing the light-emitting diodes, color reproductivity can be improved.

A backlight unit **20231** shown in FIG. **44**D has a structure in which light-emitting diodes (LEDs) **20233**, light-emitting diodes (LEDs) **20234**, and light-emitting diodes (LEDs) **20235** of R, G, and B are used as light sources. For example, among the light-emitting diodes (LEDs) **20233**, the light-emitting diodes (LEDs) **20234**, and the light-emitting diodes (LEDs) **20235** of R, G, and B, a plurality of the light-emitting diodes of a color with low emission intensity (e.g., green) are provided. By using the light-emitting diodes (LEDs) **20233**, the light-emitting diodes (LEDs) **20234**, and the light-emitting diodes (LEDs) **20235** of R, G, and B, color reproductivity can be improved. In addition, a lamp reflector **20232** is provided to efficiently reflect light from the light-emitting diodes.

Since luminance of light-emitting diodes is high, a structure using light-emitting diodes is suitable for a large display device. Since light-emitting diodes are superior in color reproductivity, an arrangement area can be reduced. Therefore, a frame of a display device can be narrowed.

By sequentially making the light-emitting diodes of R, G, and B emit light in accordance with time, color display can be performed. This is a so-called field sequential mode.

Note that a light-emitting diode which emits white light can be combined with the light-emitting diodes (LEDs) **20233**, the light-emitting diodes (LEDs) **20234**, and the light-emitting diodes (LEDs) **20235** of R, G, and B.

Note that in the case where light-emitting diodes are mounted on a large display device, the light-emitting diodes can be provided on a back side of the substrate. The light-emitting diodes of R, G, and B are sequentially provided at a predetermined interval. By providing the light-emitting diodes, color reproductivity can be improved.

FIG. **32**A shows an example of a liquid crystal display device including a so-called direct-type backlight unit **20500** and a liquid crystal panel **20505**. A direct type corresponds to a type in which a light source is provided directly under a light-emitting surface and fluorescence of the light source is emitted from the entire light-emitting surface. The direct-type backlight unit can efficiently utilize the amount of emitted light.

A backlight unit **20500** includes a diffusion plate **20501**, a light-shielding plate **20502**, a lamp reflector **20503**, and a light source **20504**.

The light source **20504** has a function of emitting light as necessary. For example, as the light source **20504**, a cold cathode fluorescent lamp, a hot cathode fluorescent lamp, a light-emitting diode, an inorganic EL element, an organic EL element, or the like is used. The lamp reflector **20503** has a function of efficiently guiding fluorescence from the light source **20504** to the diffusion plate **20501** and the light-shielding plate **20502**. The light-shielding plate **20502** has a function of reducing variations in luminance by shielding much light as light becomes more intense in accordance with provision of the light source **20504**. The diffusion plate **20501** also has a function of reducing variations in luminance.

A control circuit for controlling luminance of the light source **20504** is connected to the backlight unit **20500**. By using this control circuit, luminance of the light source **20504** can be controlled.

FIG. **32**B shows an example of a liquid crystal display device including a so-called direct-type backlight unit **20510** and a liquid crystal panel **20515**. A direct type corresponds to a type in which a light source is provided directly under a light-emitting surface and fluorescence of the light source is emitted from the entire light-emitting surface. The direct-type backlight unit can efficiently utilize the amount of emitted light.

A backlight unit **20510** includes a diffusion plate **20511**; a light-shielding plate **20512**; a lamp reflector **20513**; and a light source (R) **20514***a*, a light source (G) **20514***b*, and a light source (B) **20514***c* of R, G, and B.

Each of the light source (R) **20514***a*, the light source (G) **20514***b*, and the light source (B) **20514***c* of R, and B has a function of emitting light as necessary. For example, as each of the light source (R) **20514***a*, the light source (G) **20514***b*, and the light source (B) **20514***c*, a cold cathode fluorescent lamp, a hot cathode fluorescent lamp, a light-emitting diode, an inorganic EL element, an organic EL element, or the like is used. The lamp reflector **20513** has a function of efficiently guiding fluorescence from the light sources **20514***a* to **20514***c* to the diffusion plate **20511** and the light-shielding plate **20512**. The light-shielding plate **20512** has a function of reducing variations in brightness or luminance by shielding much light as light becomes more intense in accordance with provision of the light sources **20514***a* to **20514***c*. The diffusion plate **20511** also has a function of reducing variations in brightness or luminance.

A control circuit for controlling luminance of the light source (R) **20514***a*, the light source (G) **20514***b*, and the light source (B) **20514***c* of R, G, and B is connected to the backlight unit **20510**. By using this control circuit, luminance of the light source (R) **20514***a*, the light source (G) **20514***b*, and the light source (B) **20514***c* of R, G, and B can be controlled.

FIG. **30** shows an example of a structure of a polarizing plate (also referred to as a polarizing film).

A polarizing film **20300** includes a protective film **20301**, a substrate film **20302**, a PVA polarizing film **20303**, a substrate film **20304**, an adhesive layer **20305**, and a mold release film **20306**.

The PVA polarizing film **20303** has a function of generating light in only a certain vibration direction (linear polarized light). Specifically, the PVA polarizing film **20303** includes molecules, which function as a polarizer in which lengthwise electron density and widthwise electron density are greatly different from each other. The PVA polarizing film **20303** can generate linear polarized light by uniforming directions of the molecules in which lengthwise electron density and widthwise electron density are greatly different from each other.

For example, a high molecular film of poly vinyl alcohol is doped with an iodine compound and a PVA film is pulled in a certain direction, so that a film in which iodine molecules are aligned in a certain direction can be obtained as the PVA polarizing film **20303**. Then, light which is parallel to a major axis of the iodine molecule is absorbed by the iodine molecule. Note that a dichroic dye may be used instead of iodine for high durability use and high heat resistance use. Note that it is preferable that the dye be used for a liquid crystal display device which needs to have durability and heat resistance, such as an in-car LCD or an LCD for a projector.

When the PVA polarizing film **20303** is sandwiched by films to be base materials (the substrate film **20302** and the substrate film **20304**) from both sides, reliability can be improved. Note that the PVA polarizing film **20303** may be sandwiched by triacetylcellulose (TAC) films with high light-transmitting properties and high durability. Note that each of the substrate films and the TAC films function as protective films of polarizer included in the PVA polarizing film **20303**.

The adhesive layer **20305** which is to be attached to a glass substrate of the liquid crystal panel is attached to one of the substrate films (the substrate film **20304**). Note that the adhesive layer **20305** is formed by applying an adhesive to one of the substrate films (the substrate film **20304**). The mold release film **20306** (a separate film) is provided to the adhesive layer **20305**.

The protective film **20301** is provided to the other of the substrates films (the substrate film **20302**).

A hard coating scattering layer (an anti-glare layer) may be provided on a surface of the polarizing film **20300**. Since the surface of the hard coating scattering layer has minute unevenness formed by AG treatment and has an anti-glare function which scatters external light, reflection of external light in the liquid crystal panel can be prevented. Surface reflection can also be prevented.

Note that a treatment in which plurality of optical thin film layers having different refractive indexes are layered (also referred to as anti-reflection treatment or AR treatment) may be performed on the surface of the polarizing film **20300**. The plurality of layered optical thin film layers having different refractive indexes can reduce reflectivity on the surface by an interference effect of light.

FIGS. **31**A to **31**C each show an example of a system block of the liquid crystal display device.

In a pixel portion **20405**, signal lines **20412** which are extended from a signal line driver circuit **20403** are provided. In addition, in the pixel portion **20405**, scan lines **20410** which are extended from a scan line driver circuit **20404** are also provided. In addition, a plurality of pixels are arranged in matrix in cross regions of the signal lines **20412** and the scan lines **20410**. Note that each of the plurality of pixels includes a switching element. Therefore, voltage for controlling inclination of liquid crystal molecules can be separately input to each of the plurality of pixels. A structure in which a switching element is provided in each cross region in this manner is referred to as an active matrix type. Note that the present invention is not limited to such an active matrix type and a structure of a passive matrix type may be used. Since the passive matrix type does not have a switching element in each pixel, a process is simple.

A driver circuit portion **20408** includes a control circuit **20402**, the signal line driver circuit **20403**, and the scan line driver circuit **20404**. An image signal **20401** is input to the control circuit **20402**. The signal line driver circuit **20403** and the scan line driver circuit **20404** are controlled by the control circuit **20402** in accordance with this image signal **20401**. That is, the control circuit **20402** inputs a control signal to each of the signal line driver circuit **20403** and the scan line driver circuit **20404**. Then, in accordance with this control signal, the signal line driver circuit **20403** inputs a video signal to each of the signal lines **20412** and the scan line driver circuit **20404** inputs a scan signal to each of the scan lines **20410**. Then, the switching element included in the pixel is selected in accordance with the scan signal and the video signal is input to a pixel electrode of the pixel.

Note that the control circuit **20402** also controls a power source **20407** in accordance with the image signal **20401**. The power source **20407** includes a unit for supplying power to a lighting unit **20406**. As the lighting unit **20406**, an edge-light type backlight unit or a direct-type backlight unit can be used. Note that a front light may be used as the lighting unit **20406**. A front light corresponds to a plate-like lighting unit including a luminous body and a light conducting body, which is attached to the front surface side of a pixel portion and illuminates the whole area. By using such a lighting unit, the pixel portion can be uniformly illuminated at low power consumption.

As shown in FIG. **31**B, the scan line driver circuit **20404** includes a shift register **20441**, a level shifter **20442**, and a circuit functioning as a buffer **20443**. A control signal such as a gate start pulse (GSP) or a gate clock signal (GCK) is input to the shift register **20441**.

As shown in FIG. **31**C, the signal line driver circuit **20403** includes a shift register **20431**, a first latch **20432**, a second latch **20433**, a level shifter **20434**, and a circuit functioning as a buffer **20435**. The circuit functioning as the buffer **20435** corresponds to a circuit which has a function of amplifying a weak signal and includes an operational amplifier or the like. A control signal such as a source start pulse (SSP) or a source clock signal (SCK) is input to the level shifter **20434** and data (DATA) such as a video signal is input to the first latch **20432**. Pieces of data (DATA) can be temporally held in the second latch **20433** and are simultaneously input to the pixel portion **20405** by a latch (LAT) signal. This is referred to as line sequential driving. Therefore, when a pixel is used in which not line sequential driving but dot sequential driving is performed, the second latch can be omitted.

Note that in this embodiment mode, a known liquid crystal panel can be used for the liquid crystal panel. For example, a structure in which a liquid crystal layer is sealed between two substrates can be used as the liquid crystal panel. A transistor, a capacitor, a pixel electrode, an alignment film, or the like is formed over one of the substrates. A polarizing plate, a retardation plate, or a prism sheet may be provided on the surface opposite to a top surface of the one of the substrates. A color filter, a black matrix, a counter electrode, an alignment film, or the like is provided on the other of the substrates. A polarizing plate or a retardation plate may be provided on the surface opposite to a top surface of the other of the substrates. The color filter and the black matrix may be formed over the top surface of the one of the substrates. Note that three-dimensional display can be performed by providing a slit (a grid) on the top surface side of the one of the substrates or the surface opposite to the top surface side of the one of the substrates.

Each of the polarizing plate, the retardation plate, and the prism sheet can be provided between the two substrates. Alternatively, each of the polarizing plate, the retardation plate, and the prism sheet can be integrated with one of the two substrates.

Note that although this embodiment mode is described with reference to various drawings, the contents (or may be part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in another drawing. Further, even more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or may be part of the contents) described in each drawing of this embodiment mode can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in a drawing in another embodiment mode or embodiment. Further, even more drawings can be formed by combining each part with part of another embodiment mode or embodiment in the drawings of this embodiment mode.

This embodiment mode shows an example of an embodied case of the contents (or may be part of the contents) described in other embodiment modes and embodiments, an example of slight transformation thereof, an example of partial modification thereof, an example of improvement thereof, an example of detailed description thereof, an application example thereof, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment mode.

[Embodiment Mode 7]

In this embodiment mode, a driving method of a display device is described. In particular, a driving method of a liquid crystal display device is described.

First, overdriving is described with reference to FIGS. **33**A to **33**C. FIG. **33**A shows time change in output luminance of a display element with respect to input voltage. Time change in output luminance of the display element with respect to input voltage **30121** represented by a dashed line is as shown by output luminance **30123** represented by a dashed line similarly. That is, although voltage for obtaining intended output luminance L_o is Vi, time in accordance with response speed of the element is necessary before output luminance reaches the intended output luminance L_o when Vi is directly input as input voltage.

Overdriving is a technique for increasing this response speed. Specifically, this is a method as follows: first, Vo which is larger voltage than Vi is applied to the element for a certain time to increase response speed of the element and output luminance is made close to the intended output luminance L_o, and then, the input voltage is returned to Vi. The input voltage and the output luminance at this time are as shown by input voltage **30122** and output luminance **30124**, respectively. In the graph of the output luminance **30124**, time for reaching the intended output luminance L_o is shorter than that of the output luminance **30123**.

Note that although the case where output luminance is changed positively with respect to input voltage is described in FIG. 33A, this embodiment mode also includes the case where output luminance is changed negatively with respect to input voltage.

A circuit for realizing such driving is described with reference to FIGS. 33B and 33C. First, the case where an input image signal **30131** is a signal having an analog value (may be a discrete value) and an output image signal **30132** is also a signal having an analog value is described with reference to FIG. 33B. An overdriving circuit shown in FIG. **3313** includes an encoding circuit **30101**, a frame memory **30102**, a correction circuit **30103**, and a D/A converter circuit **30104**.

First, the input image signal **30131** is input to the encoding circuit **30101** and encoded. That is, the input image signal **30131** is converted from an analog signal into a digital signal with an appropriate bit number. After that, the converted digital signal is input to each of the frame memory **30102** and the correction circuit **30103**. An image signal of the previous frame which is held in the frame memory **30102** is input to the correction circuit **30103** at the same time. Then, in the correction circuit **30103**, an image signal corrected using an image signal of a frame and the image signal of the previous frame is output in accordance with a numeric value table which is prepared in advance. At this time, an output switching signal **30133** may be input to the correction circuit **30103** and the corrected image signal and the image signal of the frame may be switched to be output. Next, the corrected image signal or the image signal of the frame is input to the D/A converter circuit **30104**. Then, the output image signal **30132** which is an analog signal having a value in accordance with the corrected image signal or the image signal of the frame is output. In this manner, overdriving is realized.

Next, the case where the input image signal **30131** is a signal having a digital value and the output image signal **30132** is also a signal having a digital value is described with reference to FIG. 33C. An overdriving circuit shown in FIG. 33C includes a frame memory **30112** and a correction circuit **30113**.

First, the input image signal **30131** is a digital signal and is input to each of the frame memory **30112** and the correction circuit **30113**. An image signal of the previous frame which is held in the frame memory **30112** is input to the correction circuit **30113** at the same time. Then, in the correction circuit **30113**, an image signal corrected using an image signal of a frame and the image signal of the previous frame is output in accordance with a numeric value table which is prepared in advance. At this time, the output switching signal **30133** may be input to the correction circuit **30113** and the corrected image signal and the image signal of the frame may be switched to be output. In this manner, overdriving is realized.

Note that the case where the input image signal **30131** is an analog signal and the output image signal **30132** is a digital signal is included in the overdriving circuit in this embodiment mode. At this time, the D/A converter circuit **30104** is omitted from the circuit shown in FIG. 33B. In addition, the case where the input image signal **30131** is a digital signal and the output image signal **30132** is an analog signal is included in the overdriving circuit in this embodiment mode. At this time, the encoding circuit **30101** is omitted from the circuit shown in FIG. 33B.

Driving which controls a potential of a common line is described with reference to FIGS. 34A and 34B. FIG. 34A is a diagram showing a plurality of pixel circuits in which one common line is provided with respect to one scan line in a display device using a display element which has capacitive properties like a liquid crystal element. Each of the pixel circuits shown in FIG. 34A includes a transistor **30201**, an auxiliary capacitor **30202**, a display element **30203**, a video signal line **30204**, a scan line **30205**, and a common line **30206**.

A gate electrode of the transistor **30201** is electrically connected to the scan line **30205**; one of a source electrode and a drain electrode of the transistor **30201** is electrically connected to the video signal line **30204**; and the other of the source electrode and the drain electrode of the transistor **30201** is electrically connected to one of electrodes of the auxiliary capacitor **30202** and one of electrodes of the display element **30203**. In addition, the other of the electrodes of the auxiliary capacitor **30202** is electrically connected to the common line **30206**.

First, in each of pixels selected by the scan line **30205**, voltage corresponding to an image signal is applied to the display element **30203** and the auxiliary capacitor **30202** through the video signal line **30204** because the transistor **30201** is turned on. At this time, when the image signal is a signal which makes all of pixels connected to the common line **30206** display a minimum gray scale or when the image signal is a signal which makes all of the pixels connected to the common line **30206** display a maximum gray scale, it is not necessary that the image signal be written to each of the pixels through the video signal line **30204**. Voltage applied to the display element **30203** can be changed by changing a potential of the common line **30206** instead of writing the image signal through the video signal line **30204**.

Next, FIG. 34B is a diagram showing a plurality of pixel circuits in which two common lines are provided with respect to one scan line in a display device using a display element which has capacitive properties like a liquid crystal element. Each of the pixel circuits shown in FIG. 34B includes a transistor **30211**, an auxiliary capacitor **30212**, a display element **30213**, a video signal line **30214**, a scan line **30215**, a first common line **30216**, and a second common line **30217**.

A gate electrode of the transistor **30211** is electrically connected to the scan line **30215**; one of a source electrode and a drain electrode of the transistor **30211** is electrically connected to the video signal line **30214**; and the other of the source electrode and the drain electrode of the transistor **30211** is electrically connected to one of electrodes of the auxiliary capacitor **30212** and one of electrodes of the display element **30213**. In addition, the other of the electrodes of the auxiliary capacitor **30212** is electrically connected to the first common line **30216**. Further, in a pixel which is adjacent to the pixel, the other of the electrodes of the auxiliary capacitor **30212** is electrically connected to the second common line **30217**.

In the pixel circuits shown in FIG. 34B, the number of pixels which are electrically connected to one common line is small. Therefore, by changing a potential of the first common line **30216** or the second common line **30217** instead of writing an image signal through the video signal line **30214**, frequency of changing voltage applied to the display element **30213** is significantly increased. In addition, source inversion driving or dot inversion driving can be performed. By performing source inversion driving or dot inversion driving, reliability of the element can be improved and a flicker can be suppressed.

A scanning backlight is described with reference to FIGS. 35A to 35C. FIG. 35A is a view showing a scanning backlight in which cold cathode fluorescent lamps are arranged. The scanning backlight shown in FIG. 35A includes a diffusion plate **30301** and N pieces of cold cathode fluorescent lamps **30302-1** to **30302**-N. The N pieces of the cold cathode fluorescent lamps **30302-1** to **30302**-N are arranged on the back side of the diffusion plate **30301**, so that the N pieces of the cold cathode fluorescent lamps **30302-1** to **30302**-N can be scanned while luminance thereof is changed.

Change in luminance of each of the cold cathode fluorescent lamps in scanning is described with reference to FIG. **35**C. First, luminance of the cold cathode fluorescent lamp **30302-1** is changed for a certain period. After that, luminance of the cold cathode fluorescent lamp **30302-2** which is provided adjacent to the cold cathode fluorescent lamp **30302-1** is changed for the same period. In this manner, luminance is changed sequentially from the cold cathode fluorescent lamp **30302-1** to the cold cathode fluorescent lamp **30302**-N. Although luminance which is changed for a certain period is set to be lower than original luminance in FIG. **35**C, it may also be higher than original luminance. In addition, although scanning is performed from the cold cathode fluorescent lamps **30302-1** to **30302**-N, scanning may also be performed from the cold cathode fluorescent lamps **30302**-N to **30302-1**, which is in a reversed order.

By performing driving as in FIG. **35**C, average luminance of the backlight can be decreased. Therefore, power consumption of the backlight, which mainly takes up power consumption of the liquid crystal display device, can be reduced.

Note that an LED may be used as a light source of the scanning backlight. The scanning backlight in that case is as shown in FIG. **35**B. The scanning backlight shown in FIG. **35**B includes a diffusion plate **30311** and light sources **30312-1** to **30312**-N, in each of which LEDs are arranged. When the LED is used as the light source of the scanning backlight, there is an advantage in that the backlight can be thin and lightweight. In addition, there is also an advantage that a color reproduction area can be widened. Further, since the LEDs which are arranged in each of the light sources **30312-1** to **30312**-N can be similarly scanned, a dot scanning backlight can also be obtained. By using the dot scanning backlight, quality of a moving image can be further improved.

Note that when the LED is used as the light source of the backlight, driving can be performed by changing luminance as shown in FIG. **35**C.

Note that although this embodiment mode is described with reference to various drawings, the contents (or may be part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in another drawing. Further, even more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or may be part of the contents) described in each drawing of this embodiment mode can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in a drawing in another embodiment mode or embodiment. Further, even more drawings can be formed by combining each part with part of another embodiment mode or embodiment in the drawings of this embodiment mode.

This embodiment mode shows an example of an embodied case of the contents (or may be part of the contents) described in other embodiment modes and embodiments, an example of slight transformation thereof, an example of partial modification thereof, an example of improvement thereof, an example of detailed description thereof, an application example thereof, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment mode.

[Embodiment Mode 8]

In this embodiment mode, a pixel structure and an operation of a pixel which can be applied to a liquid crystal display device are described.

In this embodiment mode, as an operation mode of a liquid crystal element, a TN (twisted nematic) mode, an IPS (in-plane-switching) mode, an FFS (fringe field switching) mode, an MVA (multi-domain vertical alignment) mode, a PVA (patterned vertical alignment) mode, an ASM (axially symmetric aligned micro-cell) mode, an OCB (optical compensated birefringence) mode, an FLC (ferroelectric liquid crystal) mode, an AFLC (antiferroelectric liquid crystal) mode, or the like can be used.

FIG. **36**A shows an example of a pixel structure which can be applied to the liquid crystal display device.

A pixel **40100** includes a transistor **40101**, a liquid crystal element **40102**, and a capacitor **40103**. A gate of the transistor **40101** is connected to a wiring **40105**. A first electrode of the transistor **40101** is connected to a wiring **40104**. A second electrode of the transistor **40101** is connected to a first electrode of the liquid crystal element **40102** and a first electrode of the capacitor **40103**. A second electrode of the liquid crystal element **40102** corresponds to a counter electrode **40107**. A second electrode of the capacitor **40103** is connected to a wiring **40106**.

The wiring **40104** functions as a signal line. The wiring **40105** functions as a scan line. The wiring **40106** functions as a capacitor line. The transistor **40101** functions as a switch. The capacitor **40103** functions as a storage capacitor.

It is acceptable as long as the transistor **40101** functions as a switch, and the transistor **40101** may be either a P-channel transistor or an N-channel transistor.

A video signal is input to the wiring **40104**. A scan signal is input to the wiring **40105**. A constant potential is supplied to the wiring **40106**. Note that the scan signal is an H-level or L-level digital voltage signal. In the case where the transistor **40101** is an N-channel transistor, an H level of the scan signal is a potential which can turn on the transistor **40101** and an L level of the scan signal is a potential which can turn off the transistor **40101**. Alternatively, in the case where the transistor **40101** is a P-channel transistor, the H level of the scan signal is a potential which can turn off the transistor **40101** and the L level of the scan signal is a potential which can turn on the transistor **40101**. Note that the video signal has analog voltage. The video signal has a potential which is lower than the H level of the scan signal and higher than the L level of the scan signal. Note that the constant potential supplied to the wiring **40106** is preferably equal to a potential of the counter electrode **40107**.

Operations of the pixel **40100** are described by dividing the whole operations into the case where the transistor **40101** is on and the case where the transistor **40101** is off.

In the case where the transistor **40101** is on, the wiring **40104** is electrically connected to the first electrode (a pixel electrode) of the liquid crystal element **40102** and the first electrode of the capacitor **40103**. Therefore, the video signal is input to the first electrode (the pixel electrode) of the liquid crystal element **40102** and the first electrode of the capacitor **40103** from the wiring **40104** through the transistor **40101**. In addition, the capacitor **40103** holds a potential difference between a potential of the video signal and the potential supplied to the wiring **40106**.

In the case where the transistor **40101** is off, the wiring **40104** is not electrically connected to the first electrode (the pixel electrode) of the liquid crystal element **40102** and the first electrode of the capacitor **40103**. Therefore, each of the first electrode of the liquid crystal element **40102** and the first electrode of the capacitor **40103** is set in a floating state. Since the capacitor **40103** holds the potential difference between the potential of the video signal and the potential supplied to the wiring **40106**, each of the first electrode of the liquid crystal element **40102** and the first electrode of the capacitor **40103** holds a potential which is the same as (corresponds to) the video signal. Note that the liquid crystal element **40102** has transmissivity in accordance with the video signal.

FIG. **36**B shows an example of a pixel structure which can be applied to the liquid crystal display device. In particular, FIG. **36**B shows an example of a pixel structure which can be applied to a liquid crystal display device suitable for a horizontal electric field mode (including an IPS mode and an FFS mode).

A pixel **40110** includes a transistor **40111**, a liquid crystal element **40112**, and a capacitor **40113**. A gate of the transistor **40111** is connected to a wiring **40115**. A first electrode of the transistor **40111** is connected to a wiring **40114**. A second electrode of the transistor **40111** is connected to a first electrode of the liquid crystal element **40112** and a first electrode of the capacitor **40113**. A second electrode of the liquid crystal element **40112** is connected to a wiring **40116**. A second electrode of the capacitor **40103** is connected to the wiring **40116**.

The wiring **40114** functions as a signal line. The wiring **40115** functions as a scan line. The wiring **40116** functions as a capacitor line. The transistor **40111** functions as a switch. The capacitor **40113** functions as a storage capacitor.

It is acceptable as long as the transistor **40111** functions as a switch, and the transistor **40111** may be a P-channel transistor or an N-channel transistor.

A video signal is input to the wiring **40114**. A scan signal is input to the wiring **40115**. A constant potential is supplied to the wiring **40116**. Note that the scan signal is an H-level or L-level digital voltage signal. In the case where the transistor **40111** is an N-channel transistor, an H level of the scan signal is a potential which can turn on the transistor **40111** and an L level of the scan signal is a potential which can turn off the transistor **40111**. Alternatively, in the case where the transistor **40111** is a P-channel transistor, the H level of the scan signal is a potential which can turn off the transistor **40111** and the L level of the scan signal is a potential which can turn on the transistor **40111**. Note that the video signal has analog voltage. The video signal has a potential which is lower than the H level of the scan signal and higher than the L level of the scan signal.

Operations of the pixel **40110** are described by dividing the whole operations into the case where the transistor **40111** is on and the case where the transistor **40111** is off.

In the case where the transistor **40111** is on, the wiring **40114** is electrically connected to the first electrode (a pixel electrode) of the liquid crystal element **40112** and the first electrode of the capacitor **40113**. Therefore, the video signal is input to the first electrode (the pixel electrode) of the liquid crystal element **40112** and the first electrode of the capacitor **40113** from the wiring **40114** through the transistor **40111**. In addition, the capacitor **40113** holds a potential difference between a potential of the video signal and the potential supplied to the wiring **40116**.

In the case where the transistor **40111** is off, the wiring **40114** is not electrically connected to the first electrode (the pixel electrode) of the liquid crystal element **40112** and the first electrode of the capacitor **40113**. Therefore, each of the first electrode of the liquid crystal element **40112** and the first electrode of the capacitor **40113** is set in a floating state. Since the capacitor **40113** holds the potential difference between the potential of the video signal and the potential supplied to the wiring **40116**, each of the first electrode of the liquid crystal element **40112** and the first electrode of the capacitor **40113** holds a potential which is the same as (corresponds to) the video signal. Note that the liquid crystal element **40112** has transmissivity in accordance with the video signal.

FIG. **37** shows an example of a pixel structure which can be applied to the liquid crystal display device. In particular, FIG. **37** shows an example of a pixel structure in which an aperture ratio of a pixel can be increased by reducing the number of wirings.

FIG. **37** shows two pixels which are provided in the same column direction (a pixel **40200** and a pixel **40210**). For example, when the pixel **40200** is provided in an N-th row, the pixel **40210** is provided in an (N+1)th row.

A pixel **40200** includes a transistor **40201**, a liquid crystal element **40202**, and a capacitor **40203**. A gate of the transistor **40201** is connected to a wiring **40205**. A first electrode of the transistor **40201** is connected to a wiring **40204**. A second electrode of the transistor **40201** is connected to a first electrode of the liquid crystal element **40202** and a first electrode of the capacitor **40203**. A second electrode of the liquid crystal element **40202** corresponds to a counter electrode **40207**. A second electrode of the capacitor **40203** is connected to a wiring which is the same as a wiring connected to a gate of a transistor of the previous row.

A pixel **40210** includes a transistor **40211**, a liquid crystal element **40212**, and a capacitor **40213**. A gate of the transistor **40211** is connected to a wiring **40215**. A first electrode of the transistor **40211** is connected to the wiring **40204**. A second electrode of the transistor **40211** is connected to a first electrode of the liquid crystal element **40212** and a first electrode of the capacitor **40213**. A second electrode of the liquid crystal element **40212** corresponds to a counter electrode **40217**. A second electrode of the capacitor **40213** is connected to the wiring which is the same as the wiring connected to the gate of the transistor of the previous row (the wiring **40205**).

The wiring **40204** functions as a signal line. The wiring **40205** functions as a scan line of the N-th row. The transistor **40201** functions as a switch. The capacitor **40203** functions as a storage capacitor.

The wiring **40215** functions as a scan line of the (N+1)th row. The transistor **40211** functions as a switch. The capacitor **40213** functions as a storage capacitor.

It is acceptable as long as each of the transistor **40201** and the transistor **40211** functions as a switch, and each of the transistor **40201** and the transistor **40211** may be either a P-channel transistor or an N-channel transistor.

A video signal is input to the wiring **40204**. A scan signal (of an N-th row) is input to the wiring **40205**. A scan signal (of an (N+1)th row) is input to the wiring **40215**.

The scan signal is an H-level or L-level digital voltage signal. In the case where the transistor **40201** (or the transistor **40211**) is an N-channel transistor, an H level of the scan signal is a potential which can turn on the transistor **40201** (or the transistor **40211**) and an L level of the scan signal is a potential which can turn off the transistor **40201** (or the transistor **40211**). Alternatively, in the case where the transistor **40201** (or the transistor **40211**) is a P-channel transistor, the H level of the scan signal is a potential which can turn off the transistor **40201** (or the transistor **40211**) and the L level of the scan signal is a potential which can turn on the transistor **40201** (or the transistor **40211**). Note that the video signal has analog voltage. The video signal has a potential which is lower than the H level of the scan signal and higher than the L level of the scan signal.

Operations of the pixel **40200** are described by dividing the whole operations into the case where the transistor **40201** is on and the case where the transistor **40201** is off.

In the case where the transistor **40201** is on, the wiring **40204** is electrically connected to the first electrode (a pixel electrode) of the liquid crystal element **40202** and the first electrode of the capacitor **40203**. Therefore, the video signal is input to the first electrode (the pixel electrode) of the liquid crystal element **40202** and the first electrode of the capacitor **40203** from the wiring **40204** through the transistor **40201**. In addition, the capacitor **40203** holds a potential difference between a potential of the video signal and a potential supplied to the wiring which is the same as the wiring connected to the gate of the transistor of the previous row.

In the case where the transistor **40201** is off, the wiring **40204** is not electrically connected to the first electrode (the pixel electrode) of the liquid crystal element **40202** and the first electrode of the capacitor **40203**. Therefore, each of the first electrode of the liquid crystal element **40202** and the first electrode of the capacitor **40203** is set in a floating state. Since the capacitor **40203** holds the potential difference between the potential of the video signal and the potential of the wiring which is the same as the wiring connected to the gate of the transistor of the previous row, each of the first electrode of the liquid crystal element **40202** and the first electrode of the capacitor **40203** holds a potential which is the same as (corresponds to) the video signal. Note that the liquid crystal element **40202** has transmissivity in accordance with the video signal.

Operations of the pixel **40210** are described by dividing the whole operations into the case where the transistor **40211** is on and the case where the transistor **40211** is off.

In the case where the transistor **40211** is on, the wiring **40214** is electrically connected to the first electrode (a pixel electrode) of the liquid crystal element **40212** and the first electrode of the capacitor **40213**. Therefore, the video signal is input to the first electrode (the pixel electrode) of the liquid crystal element **40212** and the first electrode of the capacitor **40213** from the wiring **40214** through the transistor **40211**. In addition, the capacitor **40213** holds a potential difference between a potential of the video signal and a potential supplied to a wiring which is the same as the wiring connected to the gate of the transistor of the previous row (the wiring **40205**).

In the case where the transistor **40211** is off, the wiring **40214** is not electrically connected to the first electrode (the pixel electrode) of the liquid crystal element **40212** and the first electrode of the capacitor **40213**. Therefore, each of the first electrode of the liquid crystal element **40212** and the first electrode of the capacitor **40213** is set in a floating state. Since the capacitor **40103** holds the potential difference between the potential of the video signal and the potential of the wiring which is the same as the wiring connected to the gate of the transistor of the previous row (the wiring **40215**), each of the first electrode (the pixel electrode) of the liquid crystal element **40212** and the first electrode of the capacitor **40213** holds a potential which is the same as (corresponds to) the video signal. Note that the liquid crystal element **40212** has transmissivity in accordance with the video signal.

FIG. **38** shows an example of a pixel structure which can be applied to the liquid crystal display device. In particular, FIG. **38** shows an example of a pixel structure in which a viewing angle can be improved by using a subpixel.

A pixel **40320** includes a subpixel **40300** and a subpixel **40310**. Although the case in which the pixel **40320** includes two subpixels is described, the pixel **40320** may include three or more subpixels.

The subpixel **40300** includes a transistor **40301**, a liquid crystal element **40302**, and a capacitor **40303**. A gate of the transistor **40301** is connected to a wiring **40305**. A first electrode of the transistor **40301** is connected to a wiring **40304**. A second electrode of the transistor **40301** is connected to a first electrode of the liquid crystal element **40302** and a first electrode of the capacitor **40301**. A second electrode of the liquid crystal element **40302** corresponds to a counter electrode **40307**. A second electrode of the capacitor **40303** is connected to a wiring **40306**.

The subpixel **40310** includes a transistor **40311**, a liquid crystal element **40312**, and a capacitor **40313**. A gate of the transistor **40311** is connected to a wiring **40315**. A first electrode of the transistor **40311** is connected to the wiring **40304**. A second electrode of the transistor **40311** is connected to a first electrode of the liquid crystal element **40312** and a first electrode of the capacitor **40313**. A second electrode of the liquid crystal element **40312** corresponds to a counter electrode **40317**. A second electrode of the capacitor **40313** is connected to a wiring **40306**.

The wiring **40304** functions as a signal line. The wiring **40305** functions as a scan line. The wiring **40315** functions as a signal line. The wiring **40306** functions as a capacitor line. Each of the transistor **40301** and the transistor **40311** functions as a switch. Each of the capacitor **40303** and the capacitor **40313** functions as a storage capacitor.

It is acceptable as long as each of the transistor **40301** and the transistor **40311** functions as a switch, and each of the transistor **40301** and the transistor **40311** may be either a P-channel transistor or an N-channel transistor.

A video signal is input to the wiring **40304**. A scan signal is input to the wiring **40305**. A scan signal is input to the wiring **40315**. A constant potential is supplied to the wiring **40306**.

The scan signal is an H-level or L-level digital voltage signal. In the case where the transistor **40301** (or the transistor **40311**) is an N-channel transistor, an H level of the scan signal is a potential which can turn on the transistor **40301** (or the transistor **40311**) and an L level of the scan signal is a potential which can turn off the transistor **40301** (or the transistor **40311**). Alternatively, in the case where the transistor **40301** (or the transistor **40311**) is a P-channel transistor, the H level of the scan signal is a potential which can turn off the transistor **40301** (or the transistor **40311**) and the L level of the scan signal is a potential which can turn on the transistor **40301** (or the transistor **40311**). Note that the video signal has analog voltage. The video signal has a potential which is lower than the H level of the scan signal and higher than the L level of the scan signal. Note that the constant potential supplied to the wiring **40306** is preferably equal to a potential of the counter electrode **40307**.

Operations of the pixel **40320** are described by dividing the whole operations into the case where the transistor **40301** is on and the transistor **40311** is off, the case where the transistor **40301** is off and the transistor **40311** is on, and the case where the transistor **40301** and the transistor **40311** are off.

In the case where the transistor **40301** is on and the transistor **40311** is off, the wiring **40304** is electrically connected to the first electrode (a pixel electrode) of the liquid crystal element **40302** and the first electrode of the capacitor **40303** in the subpixel **40300**. Therefore, the video signal is input to the first electrode (the pixel electrode) of the liquid crystal element **40302** and the first electrode of the capacitor **40303** from the wiring **40304** through the transistor **40301**. In addition, the capacitor **40303** holds a potential difference between a potential of the video signal and a potential supplied to the wiring **40306**. At this time, the wiring **40304** is not electrically connected to the first electrode (the pixel electrode) of the liquid crystal element **40312** and the first electrode of the capacitor **40313** in the subpixel **40310**. Therefore, the video signal is not input to the subpixel **40310**.

In the case where the transistor **40301** is off and the transistor **40311** is on, the wiring **40304** is not electrically connected to the first electrode (the pixel electrode) of the liquid crystal element **40302** and the first electrode of the capacitor **40303** in the subpixel **40300**. Therefore, each of the first electrode of the liquid crystal element **40302** and the first electrode of the capacitor **40303** is set in a floating state. Since the capacitor **40303** holds the potential difference between the potential of the video signal and the potential supplied to the wiring **40306**, each of the first electrode of the liquid crystal element **40302** and the first electrode of the capacitor **40303** holds a potential which is the same as (corresponds to) the video signal. At this time, the wiring **40304** is electrically connected to the first electrode (the pixel electrode) of the liquid crystal element **40312** and the first electrode of the capacitor **40313** in the subpixel **40310**. Therefore, the video signal is input to the first electrode (the pixel electrode) of the liquid crystal element **40312** and the first electrode of the capacitor **40313** from the wiring **40304** through the transistor **40311**. In addition, the capacitor **40313** holds a potential difference between a potential of the video signal and a potential supplied to the wiring **40306**.

In the case where the transistor **40301** and the transistor **40311** are off, the wiring **40304** is not electrically connected to the first electrode (the pixel electrode) of the liquid crystal element **40302** and the first electrode of the capacitor **40303** in the subpixel **40300**. Therefore, each of the first electrode of the liquid crystal element **40302** and the first electrode of the capacitor **40303** is set in a floating state. Since the capacitor **40303** holds the potential difference between the potential of the video signal and the potential supplied to the wiring **40306**, each of the first electrode of the liquid crystal element **40302** and the first electrode of the capacitor **40303** holds a potential which is the same as (corresponds to) the video signal. Note that the liquid crystal element **40302** has transmissivity in accordance with the video signal. At this time, the wiring **40304** is not electrically connected to the first electrode (the pixel electrode) of the liquid crystal element **40312** and the first electrode of the capacitor **40313** similarly in the subpixel **40310**. Therefore, each of the first electrode of the liquid crystal element **40312** and the first electrode of the capacitor **40313** is set in a floating state. Since the capacitor **40313** holds the potential difference between the potential of the video signal and the potential of the wiring **40316**, each of the first electrode of the liquid crystal element **40312** and the first electrode of the capacitor **40313** holds a potential which is the same as (corresponds to) the video signal. Note that the liquid crystal element **40312** has transmissivity in accordance with the video signal.

A video signal input to the subpixel **40300** may be a value which is different from that of a video signal input to the subpixel **40310**. In this case, the viewing angle can be widened because alignment of liquid crystal molecules of the liquid crystal element **40302** and alignment of liquid crystal molecules of the liquid crystal element **40312** can be varied from each other.

Although this embodiment mode is described with reference to various drawings, the contents (or may be part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in another drawing. Further, even more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or may be part of the contents) described in each drawing of this embodiment mode can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in a drawing in another embodiment mode or embodiment. Further, even more drawings can be formed by combining each part with part of another embodiment mode or embodiment in the drawings of this embodiment mode.

This embodiment mode shows an example of an embodied case of the contents (or may be part of the contents) described in other embodiment modes and embodiments, an example of slight transformation thereof, an example of partial modification thereof, an example of improvement thereof, an example of detailed description thereof, an application example thereof, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment mode.

[Embodiment Mode 9]

In this embodiment mode, various liquid crystal modes are described.

First, various liquid crystal modes are described with reference to cross-sectional views.

FIGS. **39**A and **39**B are schematic views of cross sections of a TN mode.

A liquid crystal layer **50100** is held between a first substrate **50101** and a second substrate **50102** which are provided so as to be opposite to each other. A first electrode **50105** is formed on a top surface of the first substrate **50101**. A second electrode **50106** is formed on a top surface of the second substrate **50102**. A first polarizing plate **50103** is provided on a surface of the first substrate **50101**, which does not face the liquid crystal layer. A second polarizing plate **50104** is provided on a surface of the second substrate **50102**, which does not face the liquid crystal layer. Note that the first polarizing plate **50103** and the second polarizing plate **50104** are provided so as to be in a cross nicol state.

The first polarizing plate **50103** may be provided on the top surface of the first substrate **50101**. The second polarizing plate **50104** may be provided on the top surface of the second substrate **50102**.

It is acceptable as long as at least one of or both the first electrode **50105** and the second electrode **50106** have light-transmitting properties (a transmissive or reflective liquid crystal display device). Alternatively, both the first electrode **50105** and the second electrode **50106** may have light-transmitting properties, and part of one of the electrodes may have reflectivity (a semi-transmissive liquid crystal display device).

FIG. **39**A is a schematic view of a cross section in the case where voltage is applied to the first electrode **50105** and the second electrode **50106** (referred to as a vertical electric field mode). Since liquid crystal molecules are aligned longitudinally, light emitted from a backlight is not affected by birefringence of the liquid crystal molecules. In addition, since the first polarizing plate **50103** and the second polarizing plate **50104** are provided so as to be in a cross nicol state, light emitted from the backlight cannot pass through the substrate. Therefore, black display is performed.

Note that by controlling voltage applied to the first electrode **50105** and the second electrode **50106**, conditions of the liquid crystal molecules can be controlled. Therefore, since the amount of light emitted from the backlight passing through the substrate can be controlled, predetermined image display can be performed.

FIG. **39**B is a schematic view of a cross section in the case where voltage is not applied to the first electrode **50105** and the second electrode **50106**. Since the liquid crystal molecules are aligned laterally and rotated in a plane, light emitted from a backlight is affected by birefringence of the liquid crystal molecules. In addition, since the first polarizing plate **50103** and the second polarizing plate **50104** are provided so as to be in a cross nicol state, light emitted from the backlight passes through the substrate. Therefore, white display is performed. This is a so-called normally white mode.

A liquid crystal display device having a structure shown in FIG. **39**A or FIG. **39**B can perform full-color display by being provided with a color filter. The color filter can be provided on a first substrate **50101** side or a second substrate **50102** side.

It is acceptable as long as a known material is used for a liquid crystal material used for a TN mode.

FIGS. **40**A and **40**B are schematic views of cross sections of a VA mode. In the VA mode, liquid crystal molecules are aligned such that they are vertical to a substrate when there is no electric field.

A liquid crystal layer **50200** is held between a first substrate **50201** and a second substrate **50202** which are provided so as to be opposite to each other. A first electrode **50205** is formed on a top surface of the first substrate **50201**. A second electrode **50206** is formed on a top surface of the second substrate **50202**. A first polarizing plate **50203** is provided on a surface of the first substrate **50201**, which does not face the liquid crystal layer. A second polarizing plate **50204** is provided on a surface of the second substrate **50202**, which does not face the liquid crystal layer. Note that the first polarizing plate **50203** and the second polarizing plate **50204** are provided so as to be in a cross nicol state.

The first polarizing plate **50203** may be provided on the top surface of the first substrate **50201**. The second polarizing plate **50204** may be provided on the top surface of the second substrate **50202**.

It is acceptable as long as at least one of or both the first electrode **50205** and the second electrode **50206** have light-transmitting properties (a transmissive or reflective liquid crystal display device). Alternatively, both the first electrode **50205** and the second electrode **50206** may have light-transmitting properties, and part of one of the electrodes may have reflectivity (a semi-transmissive liquid crystal display device).

FIG. **40**A is a schematic view of a cross section in the case where voltage is applied to the first electrode **50205** and the second electrode **50206** (referred to as a vertical electric field mode). Since liquid crystal molecules are aligned laterally, light emitted from a backlight is affected by birefringence of the liquid crystal molecules. In addition, since the first polarizing plate **50203** and the second polarizing plate **50204** are provided so as to be in a cross nicol state, light emitted from the backlight passes through the substrate. Therefore, white display is performed.

Note that by controlling voltage applied to the first electrode **50205** and the second electrode **50206**, conditions of the liquid crystal molecules can be controlled. Therefore, since the amount of light emitted from the backlight passing through the substrate can be controlled, predetermined image display can be performed.

FIG. **40**B is a schematic view of a cross section in the case where voltage is not applied to the first electrode **50205** and the second electrode **50206**. Since liquid crystal molecules are aligned longitudinally, light emitted from a backlight is not affected by birefringence of the liquid crystal molecules. In addition, since the first polarizing plate **50203** and the second polarizing plate **50204** are provided so as to be in a cross nicol state, light emitted from the backlight does not pass through the substrate. Therefore, black display is performed. This is a so-called normally black mode.

A liquid crystal display device having a structure shown in FIG. **40**A or FIG. **40**B can perform full-color display by being provided with a color filter. The color filter can be provided on a first substrate **50201** side or a second substrate **50202** side.

It is acceptable as long as a known material is used for a liquid crystal material used for a VA mode.

FIGS. **40**C and **40**D are schematic views of cross sections of an MVA mode. In the MVA mode, viewing angle dependency of each portion is compensated by each other.

A liquid crystal layer **50210** is held between a first substrate **50211** and a second substrate **50212** which are provided so as to be opposite to each other. A first electrode **50215** is formed on a top surface of the first substrate **50211**. A second electrode **50216** is formed on a top surface of the second substrate **50212**. A first protrusion **50217** for controlling alignment is formed on the first electrode **50215**. A second protrusion **50218** for controlling alignment is formed over the second electrode **50216**. A first polarizing plate **50213** is provided on a surface of the first substrate **50211**, which does not face the liquid crystal layer. A second polarizing plate **50214** is provided on a surface of the second substrate **50212**, which does not face the liquid crystal layer. Note that the first polarizing plate **50213** and the second polarizing plate **50214** are provided so as to be in a cross nicol state.

The first polarizing plate **50213** may be provided on the top surface of the first substrate **50211**. The second polarizing plate **50214** may be provided on the top surface of the second substrate **50212**.

It is acceptable as long as at least one of or both the first electrode **50215** and the second electrode **50216** have light-transmitting properties (a transmissive or reflective liquid crystal display device). Alternatively, both the first electrode **50215** and the second electrode **50216** may have light-transmitting properties, and part of one of the electrodes may have reflectivity (a semi-transmissive liquid crystal display device).

FIG. **40**C is a schematic view of a cross section in the case where voltage is applied to the first electrode **50215** and the second electrode **50216** (referred to as a vertical electric field mode). Since liquid crystal molecules are aligned so as to tilt toward the first protrusion **50217** and the second protrusion **50218**, light emitted from a backlight is affected by birefringence of the liquid crystal molecules. In addition, since the first polarizing plate **50213** and the second polarizing plate **50214** are provided so as to be in a cross nicol state, light emitted from the backlight passes through the substrate. Therefore, white display is performed.

Note that by controlling voltage applied to the first electrode **50215** and the second electrode **50216**, conditions of the liquid crystal molecules can be controlled. Therefore, since the amount of light emitted from the backlight passing through the substrate can be controlled, predetermined image display can be performed.

FIG. **40**D is a schematic view of a cross section in the case where voltage is not applied to the first electrode **50215** and the second electrode **50216**. Since liquid crystal molecules are aligned longitudinally, light emitted from a backlight is not affected by birefringence of the liquid crystal molecules. In addition, since the first polarizing plate **50213** and the second polarizing plate **50214** are provided so as to be in a cross nicol state, light emitted from the backlight does not pass through the substrate. Therefore, black display is performed. This is a so-called normally black mode.

A liquid crystal display device having a structure shown in FIG. **40**C or FIG. **40**D can perform full-color display by being provided with a color filter. The color filter can be provided on a first substrate **50211** side or a second substrate **50212** side.

It is acceptable as long as a known material is used for a liquid crystal material used for an MVA mode.

FIGS. **41**A and **41**B are schematic views of cross sections of an OCB mode. In the OCB mode, viewing angle dependency is low because alignment of liquid crystal molecules in a liquid crystal layer can be optically compensated. This state of the liquid crystal molecules is referred to as bend alignment.

A liquid crystal layer **50300** is held between a first substrate **50301** and a second substrate **50302** which are provided so as to be opposite to each other. A first electrode **50305** is formed on a top surface of the first substrate **50301**. A second electrode **50306** is formed on a top surface of the second substrate **50302**. A first polarizing plate **50303** is provided on a surface of the first substrate **50301**, which does not face the liquid crystal layer. A second polarizing plate **50304** is provided on a surface of the second substrate **50302**, which does not face the liquid crystal layer. Note that the first polarizing plate **50303** and the second polarizing plate **50304** are provided so as to be in a cross nicol state.

The first polarizing plate **50303** may be provided on the top surface of the first substrate **50301**. The second polarizing plate **50304** may be provided on the top surface of the second substrate **50302**.

It is acceptable as long as at least one of or both the first electrode **50305** and the second electrode **50306** have light-transmitting properties (a transmissive or reflective liquid crystal display device). Alternatively, both the first electrode **50305** and the second electrode **50306** may have light-transmitting properties, and part of one of the electrodes may have reflectivity (a semi-transmissive liquid crystal display device).

FIG. **41**A is a schematic view of a cross section in the case where voltage is applied to the first electrode **50305** and the second electrode **50306** (referred to as a vertical electric field mode). Since liquid crystal molecules are aligned longitudinally, light emitted from a backlight is not affected by birefringence of the liquid crystal molecules. In addition, since the first polarizing plate **50303** and the second polarizing plate **50304** are provided so as to be in a cross nicol state, light emitted from the backlight does not pass through the substrate. Therefore, black display is performed.

Note that by controlling voltage applied to the first electrode **50305** and the second electrode **50306**, conditions of the liquid crystal molecules can be controlled. Therefore, since the amount of light emitted from the backlight passing through the substrate can be controlled, predetermined image display can be performed.

FIG. **41**B is a schematic view of a cross section in the case where voltage is not applied to the first electrode **50305** and the second electrode **50306**. Since liquid crystal molecules are in a bend alignment state, light emitted from a backlight is affected by birefringence of the liquid crystal molecules. In addition, since the first polarizing plate **50303** and the second polarizing plate **50304** are provided so as to be in a cross nicol state, light emitted from the backlight passes through the substrate. Therefore, white display is performed. This is a so-called normally white mode.

A liquid crystal display device having a structure shown in FIG. **41**A or FIG. **41**B can perform full-color display by being provided with a color filter. The color filter can be provided on a first substrate **50301** side or a second substrate **50302** side.

It is acceptable as long as a known material is used for a liquid crystal material used for an OCB mode.

FIGS. **41**C and **41**D are schematic views of cross sections of an FLC mode or an AFLC mode.

A liquid crystal layer **50310** is held between a first substrate **50311** and a second substrate **50312** which are provided so as to be opposite to each other. A first electrode **50315** is formed on a top surface of the first substrate **50311**. A second electrode **50316** is formed on a top surface of the second substrate **50312**. A first polarizing plate **50313** is provided on a surface of the first substrate **50311**, which does not face the liquid crystal layer. A second polarizing plate **50314** is provided on a surface of the second substrate **50312**, which does not face the liquid crystal layer. Note that the first polarizing plate **50313** and the second polarizing plate **50314** are provided so as to be in a cross nicol state.

The first polarizing plate **50313** may be provided on the top surface of the first substrate **50311**. The second polarizing plate **50314** may be provided on the top surface of the second substrate **50312**.

It is acceptable as long as at least one of or both the first electrode **50315** and the second electrode **50316** have light-transmitting properties (a transmissive or reflective liquid crystal display device). Alternatively, both the first electrode **50315** and the second electrode **50316** may have light-transmitting properties, and part of one of the electrodes may have reflectivity (a semi-transmissive liquid crystal display device).

FIG. **41**C is a schematic view of a cross section in the case where voltage is applied to the first electrode **50315** and the second electrode **50316** (referred to as a vertical electric field mode). Since liquid crystal molecules are aligned laterally in a direction which is deviated from a rubbing direction, light emitted from a backlight is affected by birefringence of the liquid crystal molecules. In addition, since the first polarizing plate **50313** and the second polarizing plate **50314** are provided so as to be in a cross nicol state, light emitted from the backlight passes through the substrate. Therefore, white display is performed.

Note that by controlling voltage applied to the first electrode **50315** and the second electrode **50316**, conditions of the liquid crystal molecules can be controlled. Therefore, since the amount of light emitted from the backlight passing through the substrate can be controlled, predetermined image display can be performed.

FIG. **41**D is a schematic view of a cross section in the case where voltage is not applied to the first electrode **50315** and the second electrode **50316**. Since liquid crystal molecules are aligned laterally in a rubbing direction, light emitted from a backlight is not affected by birefringence of the liquid crystal molecules. In addition, since the first polarizing plate **50313** and the second polarizing plate **50314** are provided so as to be in a cross nicol state, light emitted from the backlight does not pass through the substrate. Therefore, black display is performed. This is a so-called normally black mode.

A liquid crystal display device having a structure shown in FIG. **41**C or FIG. **41**D can perform full-color display by being provided with a color filter. The color filter can be provided on a first substrate **50311** side or a second substrate **50312** side.

It is acceptable as long as a known material is used for a liquid crystal material used for an FLC mode or an AFLC mode.

FIGS. **42**A and **42**B are schematic views of cross sections of an IPS mode. In the IPS mode, alignment of liquid crystal molecules in a liquid crystal layer can be optically compensated, the liquid crystal molecules are constantly rotated in a plane parallel to a substrate, and a horizontal electric field method in which electrodes are provided only on one substrate side is used.

A liquid crystal layer **50400** is held between a first substrate **50401** and a second substrate **50402** which are provided so as to be opposite to each other. A first electrode **50405** and a second electrode **50406** are formed on a top surface of the second substrate **50402**. A first polarizing plate **50403** is provided on a surface of the first substrate **50401**, which does not face the liquid crystal layer. A second polarizing plate **50404** is provided on a surface of the second substrate **50402**, which does not face the liquid crystal layer. Note that the first polarizing plate **50403** and the second polarizing plate **50404** are provided so as to be in a cross nicol state.

The first polarizing plate **50403** may be provided on the top surface of the first substrate **50401**. The second polarizing plate **50404** may be provided on the top surface of the second substrate **50402**.

It is acceptable as long as both the first electrode **50405** and the second electrode **50406** have light-transmitting properties. Alternatively, part of one of the first electrode **50405** and the second electrode **50406** may have reflectivity.

FIG. **42**A is a schematic view of a cross section in the case where voltage is applied to the first electrode **50405** and the second electrode **50406** (referred to as a horizontal electric field mode). Since liquid crystal molecules are aligned along a line of electric force which is deviated from a rubbing direction, light emitted from a backlight is affected by birefringence of the liquid crystal molecules. In addition, since the first polarizing plate **50403** and the second polarizing plate **50404** are provided so as to be in a cross nicol state, light emitted from the backlight passes through the substrate. Therefore, white display is performed.

Note that by controlling voltage applied to the first electrode **50405** and the second electrode **50406**, conditions of the liquid crystal molecules can be controlled. Therefore, since the amount of light emitted from the backlight passing through the substrate can be controlled, predetermined image display can be performed.

FIG. **42**B is a schematic view of a cross section in the case where voltage is not applied to the first electrode **50405** and the second electrode **50406**. Since liquid crystal molecules are aligned laterally in a rubbing direction, light emitted from a backlight is not affected by birefringence of the liquid crystal molecules. In addition, since the first polarizing plate **50403** and the second polarizing plate **50404** are provided so as to be in a cross nicol state, light emitted from the backlight does not pass through the substrate. Therefore, black display is performed. This is a so-called normally black mode.

A liquid crystal display device having a structure shown in FIG. **42**A or FIG. **42**B can perform full-color display by being provided with a color filter. The color filter can be provided on a first substrate **50401** side or a second substrate **50402** side.

It is acceptable as long as a known material is used for a liquid crystal material used for an IPS mode.

FIGS. **42**C and **42**D are schematic views of cross sections of an FFS mode. In the FFS mode, alignment of liquid crystal molecules in a liquid crystal layer can be optically compensated, the liquid crystal molecules are constantly rotated in a plane parallel to a substrate, and a horizontal electric field method in which electrodes are provided only on one substrate side is used.

A liquid crystal layer **50410** is held between a first substrate **50411** and a second substrate **50412** which are provided so as to be opposite to each other. A second electrode **50416** is formed on a top surface of the second substrate **50412**. An insulating film **50417** is formed on a top surface of the second electrode **50416**. A first electrode **50415** is formed over the insulating film **50417**. A first polarizing plate **50413** is provided on a surface of the first substrate **50411**, which does not face the liquid crystal layer. A second polarizing plate **50414** is provided on a surface of the second substrate **50412**, which does not face the liquid crystal layer. Note that the first polarizing plate **50413** and the second polarizing plate **50414** are provided so as to be in a cross nicol state.

The first polarizing plate **50413** may be provided on the top surface of the first substrate **50411**. The second polarizing plate **50414** may be provided on the top surface of the second substrate **50412**.

It is acceptable as long as at least one of or both the first electrode **50415** and the second electrode **50416** have light-transmitting properties (a transmissive or reflective liquid crystal display device). Alternatively, both the first electrode **50415** and the second electrode **50416** may have light-transmitting properties, and part of one of the electrodes may have reflectivity (a semi-transmissive liquid crystal display device).

FIG. **42**C is a schematic view of a cross section in the case where voltage is applied to the first electrode **50415** and the second electrode **50416** (referred to as a horizontal electric field mode). Since liquid crystal molecules are aligned along a line of electric force which is deviated from a rubbing direction, light emitted from a backlight is affected by birefringence of the liquid crystal molecules. In addition, since the first polarizing plate **50413** and the second polarizing plate **50414** are provided so as to be in a cross nicol state, light emitted from the backlight passes through the substrate. Therefore, white display is performed.

Note that by controlling voltage applied to the first electrode **50415** and the second electrode **50416**, conditions of the liquid crystal molecules can be controlled. Therefore, since the amount of light emitted from the backlight passing through the substrate can be controlled, predetermined image display can be performed.

FIG. **42**D is a schematic view of a cross section in the case where voltage is not applied to the first electrode **50415** and the second electrode **50416**. Since liquid crystal molecules are aligned laterally in a rubbing direction, light emitted from the backlight is not affected by birefringence of the liquid crystal molecules. In addition, since the first polarizing plate **50413** and the second polarizing plate **50414** are provided so as to be in a cross nicol state, light emitted from the backlight does not pass through the substrate. Therefore, black display is performed. This is a so-called normally black mode.

A liquid crystal display device having a structure shown in FIG. **42**C or FIG. **42**D can perform full-color display by being provided with a color filter. The color filter can be provided on a first substrate **50411** side or a second substrate **50412** side.

It is acceptable as long as a known material is used for a liquid crystal material used for an FFS mode.

Next, various liquid crystal modes are described with reference to top plan views.

FIG. **43** is a top plan view of a pixel portion to which an MVA mode is applied. In the MVA mode, viewing angle dependency of each portion is compensated by each other.

FIG. **43** shows a first pixel electrode **50501**, second pixel electrodes (**50502***a*, **50502***b*, and **50502***c*), and a protrusion **50503**. The first pixel electrode **50501** is formed over the entire surface of a counter substrate. The protrusion **50503** is formed so as to be a dogleg shape. In addition, the second pixel electrodes (**50502***a*, **50502***b*, and **50502***c*) are formed over the first pixel electrode **50501** so as to have shapes corresponding to the protrusion **50503**.

Opening portions of the second pixel electrodes (**50502***a*, **50502***b*, and **50502***c*) function like protrusions.

In the case where voltage is applied to the first pixel electrode **50501** and the second pixel electrodes (**50502***a*,

50502*b*, and **50502***c*) (referred to as a vertical electric field mode), liquid crystal molecules are aligned so as to tilt toward the opening portions of the second pixel electrodes (**50502***a*, **50502***b*, and **50502***c*) and the protrusion **50503**. Since light emitted from a backlight passes through a substrate when a pair of polarizing plates is provided so as to be in a cross nicol state, white display is performed.

Note that by controlling voltage applied to the first pixel electrode **50501** and the second pixel electrodes (**50502***a*, **50502***b*, and **50502***c*), conditions of the liquid crystal molecules can be controlled. Therefore, since the amount of light emitted from the backlight passing through the substrate can be controlled, predetermined image display can be performed.

In the case where voltage is not applied to the first pixel electrode **50501** and the second pixel electrodes (**50502***a*, **50502***b*, and **50502***c*), the liquid crystal molecules are aligned longitudinally. Since light emitted from the backlight does not pass through a panel when the pair of polarizing plates is provided so as to be in the cross nicol state, black display is performed. This is a so-called normally black mode.

It is acceptable as long as a known material is used for a liquid crystal material used for an MVA mode.

FIGS. **44**A to **44**D are top plan views of a pixel portion to which an IPS mode is applied. In the IPS mode, alignment of liquid crystal molecules in a liquid crystal layer can be optically compensated, the liquid crystal molecules are constantly rotated in a plane parallel to a substrate, and a horizontal electric field method in which electrodes are provided only on one substrate side is used.

In the IPS mode, a pair of electrodes is formed so as to have different shapes.

FIG. **44**A shows a first pixel electrode **50601** and a second pixel electrode **50602**. The first pixel electrode **50601** and the second pixel electrode **50602** are wavy shapes.

FIG. **44**B shows a first pixel electrode **50611** and a second pixel electrode **50612**. The first pixel electrode **50611** and the second pixel electrode **50612** have shapes having concentric openings.

FIG. **44**C shows a first pixel electrode **50621** and a second pixel electrode **50622**. The first pixel electrode **50621** and the second pixel electrode **50622** are comb shapes and partially overlap with each other.

FIG. **44**D shows a first pixel electrode **50631** and a second pixel electrode **50632**. The first pixel electrode **50631** and the second pixel electrode **50632** are comb shapes in which electrodes engage with each other.

In the case where voltage is applied to the first pixel electrodes (**50601**, **50611**, **50621**, and **50631**) and the second pixel electrodes (**50602**, **50612**, **50622**, and **50623**) (referred to as a horizontal electric field mode), liquid crystal molecules are aligned along a line of electric force which is deviated from a rubbing direction. Since light emitted from a backlight passes through a substrate when a pair of polarizing plates is provided so as to be in a cross nicol state, white display is performed.

Note that by controlling voltage applied to the first pixel electrodes (**50601**, **50611**, **50621**, and **50631**) and the second pixel electrodes (**50602**, **50612**, **50622**, and **50623**), conditions of the liquid crystal molecules can be controlled. Therefore, since the amount of light emitted from the backlight passing through the substrate can be controlled, predetermined image display can be performed.

In the case where voltage is not applied to the first pixel electrodes (**50601**, **50611**, **50621**, and **50631**) and the second pixel electrodes (**50602**, **50612**, **50622**, and **50623**), the liquid crystal molecules are aligned laterally in the rubbing direction. Since light emitted from the backlight does not pass through the substrate when the pair of polarizing plates is provided so as to be in the cross nicol state, black display is performed. This is a so-called normally black mode.

It is acceptable as long as a known material be used for a liquid crystal material used for an IPS mode.

FIGS. **45**A to **45**D are top plan views of a pixel portion to which an FFS mode is applied. In the FFS mode, alignment of liquid crystal molecules in a liquid crystal layer can be optically compensated, the liquid crystal molecules are constantly rotated in a plane parallel to a substrate, and a horizontal electric field method in which electrodes are provided only on one substrate side is used.

In the FFS mode, a first electrode is formed over a top surface of a second electrode so as to be various shapes.

FIG. **45**A shows a first pixel electrode **50701** and a second pixel electrode **50702**. The first pixel electrode **50701** is a bent dogleg shape. The second pixel electrode **50702** is not necessarily patterned.

FIG. **45**B shows a first pixel electrode **50711** and a second pixel electrode **50712**. The first pixel electrode **50711** is a concentric shape. The second pixel electrode **50712** is not necessarily patterned.

FIG. **45**C shows a first pixel electrode **50721** and a second pixel electrode **50722**. The first pixel electrode **50721** is a winding shape. The second pixel electrode **50722** is not necessarily patterned.

FIG. **45**D shows a first pixel electrode **50731** and a second pixel electrode **50732**. The first pixel electrode **50731** is a comb shape. The second pixel electrode **50732** is not necessarily patterned.

In the case where voltage is applied to the first pixel electrodes (**50701**, **50711**, **50721**, and **50731**) and the second pixel electrodes (**50702**, **50712**, **50722**, and **50723**) (referred to as a horizontal electric field mode), liquid crystal molecules are aligned along a line of electric force which is deviated from a rubbing direction. Since light emitted from a backlight passes through a substrate when a pair of polarizing plates is provided so as to be in a cross nicol state, white display is performed.

Note that by controlling voltage applied to the first pixel electrodes (**50701**, **50711**, **50721**, and **50731**) and the second pixel electrodes (**50702**, **50712**, **50722**, and **50723**), conditions of the liquid crystal molecules can be controlled. Therefore, since the amount of light emitted from the backlight passing through the substrate can be controlled, predetermined image display can be performed.

In the case where voltage is not applied to the first pixel electrodes (**50701**, **50711**, **50721**, and **50731**) and the second pixel electrodes (**50702**, **50712**, **50722**, and **50723**), the liquid crystal molecules are aligned laterally in the rubbing direction. Since light emitted from the backlight does not pass through the substrate when the pair of polarizing plates is provided so as to be in the cross nicol state, black display is performed. This is a so-called normally black mode.

It is acceptable as long as a known material is used for a liquid crystal material used for an FFS mode.

Although this embodiment mode is described with reference to various drawings, the contents (or may be part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in another drawing. Further, even more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or may be part of the contents) described in each drawing of this embodiment mode can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in a drawing in another embodiment mode or embodiment. Further, even more drawings can be formed by combining each part with part of another embodiment mode or embodiment in the drawings of this embodiment mode.

This embodiment mode shows an example of an embodied case of the contents (or may be part of the contents) described in other embodiment modes and embodiments, an example of slight transformation thereof, an example of partial modification thereof, an example of improvement thereof, an example of detailed description thereof, an application example thereof, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment mode.

[Embodiment Mode 10]

In this embodiment mode, a pixel structure of a display device is described. In particular, a pixel structure of a display device using an organic EL element is described.

FIG. **46**A shows an example of a top plan view (a layout diagram) of a pixel including two transistors. FIG. **46**B shows an example of a cross-sectional view along X-X' in FIG. **46**A.

FIG. **46**A shows a first transistor **60105**, a first wiring **60106**, a second wiring **60107**, a second transistor **60108**, a third wiring **60111**, a counter electrode **60112**, a capacitor **60113**, a pixel electrode **60115**, a partition wall **60116**, an organic conductive film **60117**, an organic thin film **60118**, and a substrate **60119**. Note that it is preferable that the first transistor **60105** be used as a switching transistor, the first wiring **60106** as a gate signal line, the second wiring **60107** as a source signal line, the second transistor **60108** as a driving transistor, and the third wiring **60111** as a current supply line.

A gate electrode of the first transistor **60105** is electrically connected to the first wiring **60106**. One of a source electrode and a drain electrode of the first transistor **60105** is electrically connected to the second wiring **60107**. The other of the source electrode and the drain electrode of the first transistor **60105** is electrically connected to a gate electrode of the second transistor **60108** and one electrode of the capacitor **60113**. Note that the gate electrode of the first transistor **60105** includes a plurality of gate electrodes. Accordingly, leakage current in the off state of the first transistor **60105** can be reduced.

One of a source electrode and a drain electrode of the second transistor **60108** is electrically connected to the third wiring **60111**, and the other of the source electrode and the drain electrode of the second transistor **60108** is electrically connected to the pixel electrode **60115**. Accordingly, current flowing to the pixel electrode **60115** can be controlled by the second transistor **60108**.

The organic conductive film **60117** is provided over the pixel electrode **60115**, and the organic thin film **60118** (an organic compound layer) is provided thereover. The counter electrode **60112** is provided over the organic thin film **60118** (the organic compound layer). Note that the counter electrode **60112** may be formed over the entire surface to be connected to all the pixels in common, or may be patterned using a shadow mask or the like.

Light emitted from the organic thin film **60118** (the organic compound layer) is transmitted through either the pixel electrode **60115** or the counter electrode **60112**.

In FIG. **46**B, the case where light is emitted to the pixel electrode side, that is, a side on which the transistor and the like are formed is referred to as bottom emission; and the case where light is emitted to the counter electrode side is referred to as top emission.

In the case of bottom emission, it is preferable that the pixel electrode **60115** be formed of a light-transmitting conductive film. On the other hand, in the case of top emission, it is preferable that the counter electrode **60112** be formed of a light-transmitting conductive film.

In a light-emitting device for color display, EL elements having respective light emission colors of RGB may be separately formed, or an EL element with a single color may be formed over an entire surface and light emission of RGB can be obtained by using a color filter.

Note that the structures shown in FIGS. **46**A and **46**B are examples, and various structures can be employed for a pixel layout, a cross-sectional structure, a stacking order of electrodes of an EL element, and the like, other than the structures shown in FIGS. **46**A and **46**B. Further, as a light-emitting element, various elements such as a crystalline element such as an LED, and an element formed of an inorganic thin film can be used as well as the element formed of the organic thin film shown in the drawing.

FIG. **47**A shows an example of a top plan view (a layout diagram) of a pixel including three transistors. FIG. **47**B shows an example of a cross-sectional view along X-X' in FIG. **47**A.

FIG. **47**A shows a substrate **60200**, a first wiring **60201**, a second wiring **60202**, a third wiring **60203**, a fourth wiring **60204**, a first transistor **60205**, a second transistor **60206**, a third transistor **60207**, a pixel electrode **60208**, a partition wall **60211**, an organic conductive film **60212**, an organic thin film **60213**, and a counter electrode **60214**. Note that it is preferable that the first wiring **60201** be used as a source signal line, the second wiring **60202** as a gate signal line for writing, the third wiring **60203** as a gate signal line for erasing, the fourth wiring **60204** as a current supply line, the first transistor **60205** as a switching transistor, the second transistor **60206** as an erasing transistor, and the third transistor **60207** as a driving transistor.

A gate electrode of the first transistor **60205** is electrically connected to the second wiring **60202**. One of a source electrode and a drain electrode of the first transistor **60205** is electrically connected to the first wiring **60201**. The other of the source electrode and the drain electrode of the first transistor **60205** is electrically connected to a gate electrode of the third transistor **60207**. Note that the gate electrode of the first transistor **60205** includes a plurality of gate electrodes. Accordingly, leakage current in the off state of the first transistor **60205** can be reduced.

A gate electrode of the second transistor **60206** is electrically connected to the third wiring **60203**. One of a source electrode and a drain electrode of the second transistor **60206** is electrically connected to the fourth wiring **60204**. The other of the source electrode and the drain electrode of the second transistor **60206** is electrically connected to the gate electrode of the third transistor **60207**. Note that the gate electrode of the second transistor **60206** includes a plurality of gate electrodes. Accordingly, leakage current in the off state of the second transistor **60206** can be reduced.

One of a source electrode and a drain electrode of the third transistor **60207** is electrically connected to the fourth wiring **60204**, and the other of the source electrode and the drain electrode of the third transistor **60207** is electrically connected to the pixel electrode **60208**. Accordingly, current flowing to the pixel electrode **60208** can be controlled by the third transistor **60207**.

The organic conductive film **60212** is provided over the pixel electrode **60208**, and the organic thin film **60213** (an organic compound layer) is provided thereover. The counter electrode **60214** is provided over the organic thin film **60213** (the organic compound layer). Note that the counter electrode **60214** may be formed over the entire surface to be connected to all the pixels in common, or may be patterned using a shadow mask or the like.

Light emitted from the organic thin film **60213** (the organic compound layer) is transmitted through either the pixel electrode **60208** or the counter electrode **60214**.

In FIG. **47**B, the case where light is emitted to the pixel electrode side, that is, a side on which the transistor and the like are formed is referred to as bottom emission; and the case where light is emitted to the counter electrode side is referred to as top emission.

In the case of bottom emission, it is preferable that the pixel electrode **60208** be formed of a light-transmitting conductive film. On the other hand, in the case of top emission, it is preferable that the counter electrode **60214** be formed of a light-transmitting conductive film.

In a light-emitting device for color display, EL elements having respective light emission colors of RGB may be separately formed, or an EL element with a single color may be formed over an entire surface and light emission of RGB can be obtained by using a color filter.

Note that the structures shown in FIGS. **47**A and **47**B are examples, and various structures can be employed for a pixel layout, a cross-sectional structure, a stacking order of electrodes of an EL element, and the like, other than the structures shown in FIGS. **47**A and **47**B. Further, as a light-emitting element, various elements such as a crystalline element such as an LED, and an element formed of an inorganic thin film can be used as well as the element formed of the organic thin film shown in the drawing.

FIG. **48**A shows an example of a top plan view (a layout diagram) of a pixel including four transistors. FIG. **48**B shows an example of a cross-sectional view along X-X' in FIG. **48**A.

FIG. **48**A shows a substrate **60300**, a first wiring **60301**, a second wiring **60302**, a third wiring **60303**, a fourth wiring **60304**, a first transistor **60305**, a second transistor **60306**, a third transistor **60307**, a fourth transistor **60308**, a pixel electrode **60309**, a fifth wiring **60311**, a sixth wiring **60312**, a partition wall **60321**, an organic conductive film **60322**, an organic thin film **60323**, and a counter electrode **60324**. Note that it is preferable that the first wiring **60301** be used as a source signal line, the second wiring **60302** as a gate signal line for writing, the third wiring **60303** as a gate signal line for erasing, the fourth wiring **60304** as a signal line for reverse bias, the first transistor **60305** as a switching transistor, the second transistor **60306** as an erasing transistor, the third transistor **60307** as a driving transistor, the fourth transistor **60308** as a transistor for reverse bias, the fifth wiring **60311** as a current supply line, and the sixth wiring **60312** as a power supply line for reverse bias.

A gate electrode of the first transistor **60305** is electrically connected to the second wiring **60302**. One of a source electrode and a drain electrode of the first transistor **60305** is electrically connected to the first wiring **60301**. The other of the source electrode and the drain electrode of the first transistor **60305** is electrically connected to a gate electrode of the third transistor **60307**. Note that the gate electrode of the first transistor **60305** includes a plurality of gate electrodes. Accordingly, leakage current in the off state of the first transistor **60305** can be reduced.

A gate electrode of the second transistor **60306** is electrically connected to the third wiring **60303**. One of a source electrode and a drain electrode of the second transistor **60306** is electrically connected to the fifth wiring **60311**. The other of the source electrode and the drain electrode of the second transistor **60306** is electrically connected to the gate electrode of the third transistor **60307**. Note that the gate electrode of the second transistor **60306** includes a plurality of gate electrodes. Accordingly, leakage current in the off state of the second transistor **60306** can be reduced.

One of a source electrode and a drain electrode of the third transistor **60307** is electrically connected to the fifth wiring **60311**, and the other of the source electrode and the drain electrode of the third transistor **60307** is electrically connected to the pixel electrode **60309**. Accordingly, current flowing to the pixel electrode **60309** can be controlled by the third transistor **60307**.

A gate electrode of the fourth transistor **60308** is electrically connected to the fourth wiring **60304**. One of a source electrode and a drain electrode of the fourth transistor **60308** is electrically connected to the sixth wiring **60312**. The other of the source electrode and the drain electrode of the fourth transistor **60308** is electrically connected to the pixel electrode **60309**. Accordingly, a potential of the pixel electrode **60309** can be controlled by the fourth transistor **60308**, so that reverse bias can be applied to the organic conductive film **60322** and the organic thin film **60323**. When reverse bias is applied to a light-emitting element including the organic conductive film **60322**, the organic thin film **60323**, and the like, reliability of the light-emitting element can be significantly improved.

The organic conductive film **60322** is provided over the pixel electrode **60309**, and the organic thin film **60323** (an organic compound layer) is provided thereover. The counter electrode **60324** is provided over the organic thin film **60213** (the organic compound layer). Note that the counter electrode **60324** may be formed over the entire surface to be connected to all the pixels in common, or may be patterned using a shadow mask or the like.

Light emitted from the organic thin film **60323** (the organic compound layer) is transmitted through either the pixel electrode **60309** or the counter electrode **60324**.

In FIG. **48**B, the case where light is emitted to the pixel electrode side, that is, a side on which the transistor and the like are formed is referred to as bottom emission; and the case where light is emitted to the counter electrode side is referred to as top emission.

In the case of bottom emission, it is preferable that the pixel electrode **60309** be formed of a light-transmitting conductive film. On the other hand, in the case of top emission, it is preferable that the counter electrode **60324** be formed of a light-transmitting conductive film.

In a light-emitting device for color display, EL elements having respective light emission colors of RGB may be separately formed, or an EL element with a single color may be formed over an entire surface and light emission of RGB can be obtained by using a color filter.

Note that the structures shown in FIGS. **48**A and **48**B are examples, and various structures can be employed for a pixel layout, a cross-sectional structure, a stacking order of electrodes of an EL element, and the like, other than the structures shown in FIGS. **48**A and **48**B. Further, as a light-emitting element, various elements such as a crystalline element such as an LED, and an element formed of an inorganic thin film can be used as well as the element formed of the organic thin film shown in the drawing.

Note that although this embodiment mode is described with reference to various drawings, the contents (or part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in another drawing. Further, much more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or part of the contents) described in each drawing in this embodiment mode can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in a drawing in another embodiment mode or embodiment. Further, much more drawings can be formed by combining each part in each drawing in this embodiment mode with part of another embodiment mode or embodiment.

Note that this embodiment mode shows examples of embodying, slightly transforming, partially modifying, improving, describing in detail, or applying the contents (or part of the contents) described in other embodiment modes and embodiments, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment mode.

[Embodiment Mode 11]

In this embodiment mode, a structure and an operation of a pixel in a display device are described.

FIGS. **49**A and **49**B are timing charts showing an example of digital time gray scale driving. The timing chart of FIG. **49**A shows a driving method in the case where a signal writing period (an address period) to a pixel and a light-emitting period (a sustain period) are separated.

One frame period refers to a period for fully displaying an image for one display region. One frame period includes a plurality of subframe periods, and one subframe period includes an address period and a sustain period. Address periods Ta**1** to Ta**4** indicate time for writing signals to pixels in all rows, and periods Tb**1** to Tb**4** indicate time for writing signals to pixels in one row (or one pixel). Sustain periods Ts**1** to Ts**4** indicate time for maintaining a lighting state or a non-lighting state in accordance with a video signal written to the pixel, and a ratio of the length of the sustain periods is set to satisfy Ts**1**:Ts**2**:Ts**3**:Ts**4**=$2^3:2^2:2^1:2^0$=8:4:2:1. A gray scale is expressed depending on in which sustain period light emission is performed.

An operation is described. First, in the address period Ta**1**, pixel selection signals are sequentially input to scan lines from a first row, and a pixel is selected. Then, while the pixel is selected, a video signal is input to the pixel from a signal line. Then, when the video signal is written to the pixel, the pixel maintains the signal until a signal is input again. Lighting and non-lighting of each pixel in the sustain period Ts**1** are controlled by the written video signal. Similarly, in the address periods Ta**2**, Ta**1**, and Ta**4**, a video signal is input to pixels, and lighting and non-lighting of each pixel in the sustain periods Ts**2**, Ts**3**, and Ts**4** are controlled by the video signal. Then, in each subframe period, a pixel to which a signal for not lighting in the address period and for lighting when the sustain period starts after the address period ends is written is lit.

Here, the i-th pixel row is described with reference to FIG. **49**B. First, in the address period Ta**1**, pixel selection signals are input to scan lines from a first row, and in a period Tb**1** (i) in the address period Ta**1**, a pixel in the i-th row is selected. Then, while the pixel in the i-th row is selected, a video signal is input to the pixel in the i-th row from a signal line. Then, when the video signal is written to the pixel in the i-th row, the pixel in the i-th row maintains the signal until a signal is input again. Lighting and non-lighting of the pixel in the i-th row in the sustain period Ts**1** are controlled by the written video signal. Similarly, in the address periods Ta**2**, Ta**3**, and Ta**4**, a video signal is input to the pixel in the i-th row, and lighting and non-lighting of the pixel in the i-th row in the sustain periods Ts**2**, Ts**3**, and Ts**4** are controlled by the video signal. Then, in each subframe period, a pixel to which a signal for not lighting in the address period and for lighting when the sustain period starts after the address period ends is written is lit.

Here, the case where a 4-bit gray scale is expressed is described here; however, the number of bits and the number of gray scales are not limited thereto. Note that lighting is not needed to be performed in order of Ts**1**, Ts**2**, Ts**3**, and Ts**4**, and the order may be random or light may be emitted by dividing the whole period into a plurality of periods. A ratio of lighting time of Ts**1**, Ts**2**, Ts**3**, and Ts**4** is not needed to be a power of two, and may be the same length or slightly different from a power of two.

Next, a driving method in the case where a period for writing a signal to a pixel (an address period) and a light-emitting period (a sustain period) are not separated is described. That is, a pixel in a row in which a writing operation of a video signal is completed maintains the signal until another signal is written to the pixel (or the signal is erased). A period between the writing operation and writing of another signal to the pixel is referred to as data holding time. In the data holding time, the pixel is lit or not lit in accordance with the video signal written to the pixel. The same operations are performed until the last row, and the address period ends. Then, an operation proceeds to a signal writing operation of the next subframe period sequentially from a row in which the data holding time ends.

As described above, in the case of a driving method in which a pixel is immediately lit or not lit in accordance with a video signal written to the pixel when the signal writing operation is completed and the data holding time starts, signals cannot be input to two rows at the same time. Accordingly, address periods need to be prevented from overlapping, so that the data holding time cannot be made shorter. As a result, it is difficult to perform high-level gray scale display.

Thus, the data holding time is set to be shorter than the address period by provision of an erasing period. A driving method in the case where the data holding time shorter than the address period is set by provision of an erasing period is described with reference to FIG. **50**A.

First, in the address period Ta**1**, pixel scan signals are input to scan lines from a first row, and a pixel is selected. Then, while the pixel is selected, a video signal is input to the pixel from a signal line. Then, when the video signal is written to the pixel, the pixel maintains the signal until a signal is input again. Lighting and non-lighting of the pixel in the sustain period Ts**1** are controlled by the written video signal. In a row in which a writing operation of a video signal is completed, a pixel is immediately lit or not lit in accordance with the written video signal. The same operations are performed until the last row, and the address period Ta**1** ends. Then, an operation proceeds to a signal writing operation of the next subframe period sequentially from a row in which the data holding time ends. Similarly, in the address periods Ta**2**, Ta**3**, and Ta**4**, a video signal is input to the pixel, and lighting and non-lighting of the pixel in the sustain periods Ts**2**, Ts**3**, and Ts**4** are controlled by the video signal. The end of the sustain period Ts**4** is set by the start of an erasing operation. This is because when a signal written to a pixel is erased in an erasing time Te of each row, the pixel is forced to be not lit regardless of the video signal written to the pixel in the address period until another signal is written to the pixel. That is, the data holding time ends from a pixel in which the erasing time Te starts.

Here, the i-th pixel row is described with reference to FIG. **50**B. In the address period Ta**1**, pixel scan signals are input to scan lines from a first row, and a pixel is selected. Then, in the period Tb**1** (i), while the pixel in the i-th row is selected, a video signal is input to the pixel in the i-th row. Then, when the video signal is written to the pixel in the i-th row, the pixel in the i-th row maintains the signal until a signal is input again. Lighting and non-lighting of the pixel in the i-th row in a sustain period Ts**1** (i) are controlled by the written video signal. That is, the pixel in the i-th row is immediately lit or not lit in accordance with the video signal written to the pixel after the writing operation of the video signal to the i-th row is completed. Similarly, in the address periods Ta**2**, Ta**3**, and Ta**4**, a video signal is input to the pixel in the i-th row, and lighting and non-lighting of the pixel in the i-th row in the sustain periods Ts**2**, Ts**3**, and Ts**4** are controlled by the video signal. The end of a sustain period Ts**4** (i) is set by the start of an erasing operation. This is because the pixel is forced to be not lit regardless of the video signal written to the pixel in the i-th row in an erasing time Te(i) in the i-th row. That is, the data holding time of the pixel in the i-th row ends when the erasing time Te(i) starts.

Thus, a display device with a high-level gray scale and a high duty ratio (a ratio of a lighting period in one frame period) can be provided, in which data holding time is shorter than an address period without separating the address period and a sustain period. Since instantaneous luminance can be lowered, reliability of a display element can be improved.

Here, the case where a 4-bit gray scale is expressed is described here; however, the number of bits and the number of gray scales are not limited thereto. Note that lighting is not needed to be performed in order of Ts**1** , Ts**2**, Ts**3**, and Ts**4**, and the order may be random or light may be emitted by dividing the whole period into a plurality of periods. A ratio of lighting time of Ts**1**, Ts**2**, Ts**3**, and Ts**4** is not needed to be a power of two, and may be the same length or slightly different from a power of two.

Next, a structure and an operation of a pixel to which digital time gray scale driving can be applied are described.

FIG. **51** shows an example of a pixel structure to which digital time gray scale driving can be applied.

A pixel **80300** includes a switching transistor **80301**, a driving transistor **80302**, a light-emitting element **80304**, and a capacitor **80303**. A gate of the switching transistor **80301** is connected to a scan line **80306**, a first electrode (one of a source electrode and a drain electrode) of the switching transistor **80301** is connected to a signal line **80305**, and a second electrode (the other of the source electrode and the drain electrode) of the switching transistor **80301** is connected to a gate of the driving transistor **80302**. The gate of the driving transistor **80302** is connected to a power supply line **80307** through the capacitor **80303**, a first electrode of the driving transistor **80302** is connected to the power supply line **80307**, and a second electrode of the driving transistor **80302** is connected to a first electrode (a pixel electrode) of the light-emitting element **80304**. A second electrode of the light-emitting element **80304** corresponds to a common electrode **80308**.

Note that the second electrode (the common electrode **80308**) of the light-emitting element **80304** is set to have a low power supply potential. A low power supply potential refers to a potential satisfying (the low power supply potential)<(a high power supply potential) based on the high power supply potential set to the power supply line **80307**. As the low power supply potential, GND, 0 V, or the like may be set, for example. In order to make the light-emitting element **80304** emit light by applying a potential difference between the high power supply potential and the low power supply potential to the light-emitting element **80304** so that current is supplied to the light-emitting element **80304**, each of the potentials is set so that the potential difference between the high power supply potential and the low power supply potential is equal to or higher than forward threshold voltage.

Note that gate capacitance of the driving transistor **80302** may be used as a substitute for the capacitor **80303**, so that the capacitor **80303** can be omitted. The gate capacitance of the driving transistor **80302** may be formed in a region where a source region, a drain region, an LDD region, or the like overlaps with the gate electrode. Alternatively, capacitance may be formed between a channel formation region and the gate electrode.

When a pixel is selected by the scan line **80306**, that is, when the switching transistor **80301** is turned on, a video signal is input to the pixel from the signal line **80305**. Then, a charge for voltage corresponding to the video signal is stored in the capacitor **80303**, and the capacitor **80303** maintains the voltage. The voltage is voltage between the gate and the first electrode of the driving transistor **80302** and corresponds to gate-source voltage Vgs of the driving transistor **80302**.

In general, an operation region of a transistor can be divided into a linear region and a saturation region. When drain-source voltage is denoted by Vds, gate-source voltage is denoted by Vgs, and threshold voltage is denoted by Vth, a boundary between the linear region and the saturation region sets so as to satisfy (Vgs−Vth)=Vds. In the case where (Vgs−Vth)>Vds is satisfied, the transistor operates in a linear region, and a current value is determined in accordance with the level of Vds and Vgs. On the other hand, in the case where (Vgs−Vth)<Vds is satisfied, the transistor operates in a saturation region and ideally, a current value hardly changes even when Vds changes. That is, the current value is determined only by the level of Vgs.

Here, in the case of a voltage-input voltage driving method, a video signal is input to the gate of the driving transistor **80302** so that the driving transistor **80302** is in either of two states of being sufficiently turned on and turned off. That is, the driving transistor **80302** operates in a linear region.

Thus, when a video signal which makes the driving transistor **80302** turned on is input, a power supply potential VDD set to the power supply line **80307** without change is ideally set to the first electrode of the light-emitting element **80304**.

That is, ideally, constant voltage is applied to the light-emitting element **80304** to obtain constant luminance from the light-emitting element **80304**. Then, a plurality of subframe periods are provided in one frame period. A video signal is written to a pixel in each subframe period, lighting and non-lighting of the pixel are controlled in each subframe period, and a gray scale is expressed by the sum of lighting subframe periods.

Note that when the video signal by which the driving transistor **80302** operates in a saturation region is input, current can be supplied to the light-emitting element **80304**. When the light-emitting element **80304** is an element luminance of which is determined in accordance with current, luminance decay due to deterioration of the light-emitting element **80304** can be suppressed. Further, when the video signal is an analog signal, current in accordance with the video signal can be supplied to the light-emitting element **80304**. In this case, analog gray scale driving can be performed.

FIG. **52** shows another example of a pixel structure to which digital time gray scale driving can be applied.

A pixel **80400** includes a switching transistor **80401**, a driving transistor **80402**, a capacitor **80403**, a light-emitting element **80404**, and a rectifying element **80409**. A gate of the switching transistor **80401** is connected to a first scan line

80406, a first electrode (one of a source electrode and a drain electrode) of the switching transistor **80401** is connected to a signal line **80405**, and a second electrode (the other of the source electrode and the drain electrode) of the switching transistor **80401** is connected to a gate of the driving transistor **80402**. The gate of the driving transistor **80402** is connected to a power supply line **80407** through the capacitor **80403**, and is also connected to a second scan line **80410** through the rectifying element **80409**. A first electrode of the driving transistor **80402** is connected to the power supply line **80407**, and a second electrode of the driving transistor **80402** is connected to a first electrode (a pixel electrode) of the light-emitting element **80404**. A second electrode of the light-emitting element **80404** corresponds to a common electrode **80408**.

The second electrode (the common electrode **80408**) of the light-emitting element **80404** is set to have a low power supply potential. Note that a low power supply potential refers to a potential satisfying (the low power supply potential)<(a high power supply potential) based on the high power supply potential set to the power supply line **80407**. As the low power supply potential, GND, 0 V, or the like may be set, for example. In order to make the light-emitting element **80404** emit light by applying a potential difference between the high power supply potential and the low power supply potential to the light-emitting element **80404** so that current is supplied to the light-emitting element **80404**, each of the potentials is set so that the potential difference between the high power supply potential and the low power supply potential is equal to or higher than forward threshold voltage.

Note that gate capacitance of the driving transistor **80402** may be used as a substitute for the capacitor **80403**, so that the capacitor **80403** can be omitted. The gate capacitance of the driving transistor **80402** may be formed in a region where a source region, a drain region, an LDD region, or the like overlaps with the gate electrode. Alternatively, capacitance may be formed between a channel formation region and the gate electrode.

As the rectifying element **80409**, a diode-connected transistor can be used. A PN junction diode, a PIN junction diode, a Schottky diode, a diode formed of a carbon nanotube, or the like may be used other than a diode-connected transistor. A diode-connected transistor may be an n-channel transistor or a p-channel transistor.

The pixel **80400** is such that the rectifying element **80409** and the second scan line **80410** are added to the pixel shown in FIG. **51**. Accordingly, the switching transistor **80401**, the driving transistor **80402**, the capacitor **80403**, the light-emitting element **80404**, the signal line **80405**, the first scan line **80406**, the power supply line **80407**, and the common electrode **80408** shown in FIG. **52** correspond to the switching transistor **80301**, the driving transistor **80302**, the capacitor **80303**, the light-emitting element **80304**, the signal line **80305**, the scan line **80306**, the power supply line **80307**, and the common electrode **80308** shown in FIG. **51**. Accordingly, a writing operation and a light-emitting operation in FIG. **52** are similar to those described in FIG. **51**, so that description thereof is omitted.

An erasing operation is described. In the erasing operation, an H-level signal is input to the second scan line **80410**. Thus, current is supplied to the rectifying element **80409**, and a gate potential of the driving transistor **80402** held by the capacitor **80403** can be set to a certain potential. That is, the potential of the gate of the driving transistor **80402** is set to a certain value, and the driving transistor **80402** can be forced to be turned off regardless of a video signal written to the pixel.

Note that an L-level signal input to the second scan line **80410** has a potential such that current is not supplied to the rectifying element **80409** when a video signal for non-lighting is written to a pixel. An H-level signal input to the second scan line **80410** has a potential such that a potential to turn off the driving transistor **80302** can be set to the gate regardless of a video signal written to a pixel.

FIG. **53** shows another example of a pixel structure to which digital time gray scale driving can be applied.

A pixel **80500** includes a switching transistor **80501**, a driving transistor **80502**, a capacitor **80503**, a light-emitting element **80504**, and an erasing transistor **80509**. A gate of the switching transistor **80501** is connected to a first scan line **80506**, a first electrode (one of a source electrode and a drain electrode) of the switching transistor **80501** is connected to a signal line **80505**, and a second electrode (the other of the source electrode and the drain electrode) of the switching transistor **80501** is connected to a gate of the driving transistor **80502**. The gate of the driving transistor **80502** is connected to a power supply line **80507** through the capacitor **80503**, and is also connected to a first electrode of the erasing transistor **80509**. A first electrode of the driving transistor **80502** is connected to the power supply line **80507**, and a second electrode of the driving transistor **80502** is connected to a first electrode (a pixel electrode) of the light-emitting element **80504**. A gate of the erasing transistor **80509** is connected to a second scan line **80510**, and a second electrode of the erasing transistor **80509** is connected to the power supply line **80507**. A second electrode of the light-emitting element **80504** corresponds to a common electrode **80508**.

The second electrode (the common electrode **80508**) of the light-emitting element **80504** is set to have a low power supply potential. Note that a low power supply potential refers to a potential satisfying (the low power supply potential)<(a high power supply potential) based on the high power supply potential set to the power supply line **80507**. As the low power supply potential, GND, 0 V, or the like may be set, for example. In order to make the light-emitting element **80504** emit light by applying a potential difference between the high power supply potential and the low power supply potential to the light-emitting element **80504** so that current is supplied to the light-emitting element **80504**, each of the potentials is set so that the potential difference between the high power supply potential and the low power supply potential is equal to or higher than forward threshold voltage.

Note that gate capacitance of the driving transistor **80502** may be used as a substitute for the capacitor **80503**, so that the capacitor **80503** can be omitted. The gate capacitance of the driving transistor **80502** may be formed in a region where a source region, a drain region, an LDD region, or the like overlaps with the gate electrode. Alternatively, capacitance may be formed between a channel formation region and the gate electrode.

The pixel **80500** is such that the erasing transistor **80509** and the second scan line **80510** are added to the pixel shown in FIG. **51**. Accordingly, the switching transistor **80501**, the driving transistor **80502**, the capacitor **80503**, the light-emitting element **80504**, the signal line **80505**, the first scan line **80506**, the power supply line **80507**, and the common electrode **80508** shown in FIG. **53** correspond to the switching transistor **80301**, the driving transistor **80302**, the capacitor **80303**, the light-emitting element **80304**, the signal line **80305**, the scan line **80306**, the power supply line **80307**, and the common electrode **80308** shown in FIG. **51**. Accordingly, a writing operation and a light-emitting operation in FIG. **53** are similar to those described in FIG. **51**, so that description thereof is omitted.

An erasing operation is described. In the erasing operation, an H-level signal is input to the second scan line **80510**. Thus, the erasing transistor **80509** is turned on, and the gate and the first electrode of the driving transistor **80502** can be made to have the same potential. That is, Vgs of the driving transistor **80502** can be 0 V. Accordingly, the driving transistor **80502** can be forced to be turned off.

Next, a structure and an operation of a pixel called a threshold voltage compensation pixel are described. A threshold voltage compensation pixel can be applied to digital time gray scale driving and analog gray scale driving.

FIG. **54** shows an example of a structure of a pixel called a threshold voltage compensation pixel.

The pixel shown in FIG. **54** includes a driving transistor **80600**, a first switch **80601**, a second switch **80602**, a third switch **80603**, a first capacitor **80604**, a second capacitor **80605**, and a light-emitting element **80620**. A gate of the driving transistor **80600** is connected to a signal line **80611** through the first capacitor **80604** and the first switch **80601** in this order. Further, the gate of the driving transistor **80600** is connected to a power supply line **80612** through the second capacitor **80605**. A first electrode of the driving transistor **80600** is connected to the power supply line **80612**. A second electrode of the driving transistor **80600** is connected to a first electrode of the light-emitting element **80620** through the third switch **80603**. Further, the second electrode of the driving transistor **80600** is connected to the gate of the driving transistor **80600** through the second switch **80602**. A second electrode of the light-emitting element **80620** corresponds to a common electrode **80621**.

The second electrode of the light-emitting element **80620** is set to a low power supply potential. Note that a low power supply potential refers to a potential satisfying (the low power supply potential)<(a high power supply potential) based on the high power supply potential set to the power supply line **80612**. As the low power supply potential, GND, 0 V, or the like may be set, for example. In order to make the light-emitting element **80620** emit light by applying a potential difference between the high power supply potential and the low power supply potential to the light-emitting element **80620** so that current is supplied to the light-emitting element **80620**, each of the potentials is set so that the potential difference between the high power supply potential and the low power supply potential is equal to or higher than forward threshold voltage. Note that gate capacitance of the driving transistor **80600** may be used as a substitute for the second capacitor **80605**, so that the second capacitor **80605** can be omitted. The gate capacitance of the driving transistor **80600** may be formed in a region where a source region, a drain region, an LDD region, or the like overlaps with the gate electrode. Alternatively, capacitance may be formed between a channel formation region and the gate electrode. Note that on/off of the first switch **80601**, the second switch **80602**, and the third switch **80603** is controlled by a first scan line **80613**, a second scan line **80615**, and a third scan line **80614**, respectively.

A method for driving the pixel shown in FIG. **54** is described in which an operation period is divided into an initialization period, a data writing period, a threshold detecting period, and a light-emitting period.

In the initialization period, the second switch **80602** and the third switch **80603** are turned on. Then, a potential of the gate of the driving transistor **80600** is lower than at least a potential of the power supply line **80612**. At this time, the first switch **80601** may be in an on state or an off state. Note that the initialization period is not necessarily required.

In the threshold detecting period, a pixel is selected by the first scan line **80613**. That is, the first switch **80601** is turned on, and constant voltage is input from the signal line **80611**. At this time, the second switch **80602** is turned on and the third switch **80603** is turned off. Accordingly, the driving transistor **80600** is diode-connected, and the second electrode and the gate of the driving transistor **80600** are placed in a floating state. Then, a potential of the gate of the driving transistor **80600** is a value obtained by subtracting threshold voltage of the driving transistor **80600** from the potential of the power supply line **80612**. Thus, the threshold voltage of the driving transistor **80600** is held in the first capacitor **80604**. A potential difference between the potential of the gate of the driving transistor **80600** and the constant voltage input from the signal line **80611** is held in the second capacitor **80605**.

In the data writing period, a video signal (voltage) is input from the signal line **80611**. At this time, the first switch **80601** is kept on, the second switch **80602** is turned off, and the third switch **80603** is kept off. Since the gate of the driving transistor **80600** is in a floating state, the potential of the gate of the driving transistor **80600** changes depending on a potential difference between the constant voltage input from the signal line **80611** in the threshold detecting period and the video signal input from the signal line **80611** in the data writing period. For example, when (a capacitance value of the first capacitor **80604**)<<(a capacitance value of the second capacitor **80605**) is satisfied, the potential of the gate of the driving transistor **80600** in the data writing period is approximately equal to the sum of a potential difference (the amount of change) between the potential of the signal line **80611** in the threshold detecting period and the potential of the signal line **80611** in the data writing period; and a value obtained by subtracting the threshold voltage of the driving transistor **80600** from the potential of the power supply line **80612**. That is, the potential of the gate of the driving transistor **80600** becomes a potential obtained by correcting the threshold voltage of the driving transistor **80600**.

In the light-emitting period, current in accordance with a potential difference (Vgs) between the gate of the driving transistor **80600** and the power supply line **80612** is supplied to the light-emitting element **80620**. At this time, the first switch **80601** is turned off, the second switch **80602** is kept off, and the third switch **80603** is turned on. Note that current flowing to the light-emitting element **80620** is constant regardless of the threshold voltage of the driving transistor **80600**.

Note that a pixel structure of the present invention is not limited to that shown in FIG. **54**. For example, a switch, a resistor, a capacitor, a transistor, a logic circuit, or the like may be added to the pixel shown in FIG. **54**. For example, the second switch **80602** may include a p-channel transistor or an n-channel transistor, the third switch **80603** may include a transistor with polarity different from that of the second switch **80602**, and the second switch **80602** and the third switch **80603** may be controlled by the same scan line.

A structure and an operation of a pixel d a current input pixel are described. A current input pixel can be applied to digital gray scale driving and analog gray scale driving.

FIG. **55** shows an example of a structure of a current input pixel.

The pixel shown in FIG. **55** includes a driving transistor **80700**, a first switch **80701**, a second switch **80702**, a third switch **80703**, a capacitor **80704**, and a light-emitting element **80730**. A gate of the driving transistor **80700** is connected to a signal line **80711** through the second switch **80702** and the first switch **80701** in this order. Further, the gate of the driving transistor **80700** is connected to a power supply line **80712** through the capacitor **80704**. A first electrode of the driving transistor **80700** is connected to the power supply line **80712**. A second electrode of the driving transistor **80700** is connected to the signal line **80711** through the first switch **80701**. Further, the second electrode of the driving transistor **80700** is connected to a first electrode of the light-emitting element **80730** through the third switch **80703**. A second electrode of the light-emitting element **80730** corresponds to a common electrode **80731**.

The second electrode of the light-emitting element **80730** is set to a low power supply potential. Note that a low power supply potential refers to a potential satisfying (the low power supply potential)<(a high power supply potential) based on the high power supply potential set to the power supply line **80712**. As the low power supply potential, GND, 0 V, or the like may be set, for example. In order to make the light-emitting element **80730** emit light by applying a potential difference between the high power supply potential and the low power supply potential to the light-emitting element **80730** so that current is supplied to the light-emitting element **80730**, each of the potentials is set so that the potential difference between the high power supply potential and the low power supply potential is equal to or higher than forward threshold voltage. Note that gate capacitance of the driving transistor **80700** may be used as a substitute for the capacitor **80704**, so that the capacitor **80704** can be omitted. The gate capacitance of the driving transistor **80700** may be formed in a region where a source region, a drain region, an LDD region, or the like overlaps with the gate electrode. Alternatively, capacitance may be formed between a channel formation region and the gate electrode. Note that on/off of the first switch **80701**, the second switch **80702**, and the third switch **80703** is controlled by a first scan line **80713**, a second scan line **80714**, and a third scan line **80715**, respectively.

A method for driving the pixel shown in FIG. **55** is described in which an operation period is divided into a data writing period and a light-emitting period.

In the data writing period, a pixel is selected by the first scan line **80713**. That is, the first switch **80701** is turned on, and current is input as a video signal from the signal line **80711**. At this time, the second switch **80702** is turned on and the third switch **80703** is turned off. Accordingly, a potential of the gate of the driving transistor **80700** becomes a potential in accordance with the video signal. That is, voltage between the gate electrode and the source electrode of the driving transistor **80700**, which is such that the driving transistor **80700** supplies the same current as the video signal, is held in the capacitor **80704**.

Next, in the light-emitting period, the first switch **80701** and the second switch **80702** are turned off, and the third switch **80703** is turned on. Thus, current with the same value as the video signal is supplied to the light-emitting element **80730**.

Note that the present invention is not limited to the pixel structure shown in FIG. **55**. For example, a switch, a resistor, a capacitor, a transistor, a logic circuit, or the like may be added to the pixel shown in FIG. **55**. For example, the first switch **80701** may include a p-channel transistor or an n-channel transistor, the second switch **80702** may include a transistor with the same polarity as that of the first switch **80701**, and the first switch **80701** and the second switch **80702** may be controlled by the same scan line. The second switch **80702** may be provided between the gate of the driving transistor **80700** and the signal line **80711**.

Note that although this embodiment mode is described with reference to various drawings, the contents (or part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in another drawing. Further, much more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or part of the contents) described in each drawing in this embodiment mode can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in a drawing in another embodiment mode or embodiment. Further, much more drawings can be formed by combining each part in each drawing in this embodiment mode with part of another embodiment mode or embodiment.

Note that this embodiment mode shows examples of embodying, slightly transforming, partially modifying, improving, describing in detail, or applying the contents (or part of the contents) described in other embodiment modes and embodiments, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment mode.

[Embodiment Mode 12]

In this embodiment mode, a structure and a manufacturing method of a transistor are described.

FIGS. **56**A to **56**G show examples of structures and manufacturing methods of transistors included in a display device to which the present invention can be applied. FIG. **56**A shows structure examples of transistors included in the display device to which the present invention can be applied. FIGS. **56**B to **56**G show examples of manufacturing methods of the transistors included in the display device to which the present invention can be applied.

Note that the structure and the manufacturing method of the transistors included in the display device to which the present invention can be applied are not limited to those shown in FIGS. **56**A to **56**G, and various structures and manufacturing methods can be employed.

First, structure examples of transistors included in the display device to which the present invention can be applied are described with reference to FIG. **56**A. FIG. **56**A is a cross-sectional view of a plurality of transistors each having a different structure. Here, in FIG. **56**A, the plurality of transistors each having a different structure are juxtaposed, which is for describing structures of the transistors. Accordingly, the transistors are not needed to be actually juxtaposed as shown in FIG. **56**A and can be separately formed as needed.

Next, characteristics of each layer forming the transistor included in the display device to which the present invention can be applied are described.

A substrate **110111** can be a glass substrate using barium borosilicate glass, aluminoborosilicate glass, or the like, a quartz substrate, a ceramic substrate, a metal substrate containing stainless steel, or the like. Further, a substrate formed of plastics typified by polyethylene terephthalate (PET), polyethylene naphthalate (PEN), or polyethersulfone (PES), or a substrate formed of a flexible synthetic resin such as acrylic can also be used. By using a flexible substrate, a display device capable of being bent can be formed. A flexible substrate has no strict limitations on the area or the shape of the substrate. Accordingly, for example, when a substrate having a rectangular shape, each side of which is 1 meter or more, is used as the substrate **110111**, productivity can be significantly improved. Such an advantage is highly favorable as compared with the case where a circular silicon substrate is used.

An insulating film **110112** functions as a base film and is provided to prevent alkali metal such as Na or alkaline earth metal from the substrate **110111** from adversely affecting characteristics of a semiconductor element. The insulating film **110112** can have a single-layer structure or a stacked-layer structure of an insulating film containing oxygen or nitrogen, such as silicon oxide (SiO_x), silicon nitride (SiN_x), silicon oxynitride (SiO_xN_y) (x>y), or silicon nitride oxide (SiN_xO_y) (x>y). For example, when the insulating film **110112** is provided to have a two-layer structure, it is preferable that a silicon nitride oxide film be used as a first insulating film and a silicon oxynitride film be used as a second insulating film. Further, when the insulating film **110112** is provided to have a three-layer structure, it is preferable that a silicon oxynitride film be used as a first insulating film, a silicon nitride oxide film be used as a second insulating film, and a silicon oxynitride film be used as a third insulating film.

Semiconductor layers **110113**, **110114**, and **110115** can be formed using an amorphous semiconductor or a semi-amorphous semiconductor (SAS). Alternatively, a polycrystalline semiconductor layer may be used. SAS is a semiconductor having an intermediate structure between amorphous and crystalline (including single crystal and polycrystalline) structures and having a third state which is stable in free energy. Moreover, SAS includes a crystalline region with a short-range order and lattice distortion. A crystalline region of 0.5 to 20 nm can be observed at least in part of a film. When silicon is contained as a main component, Raman spectrum shifts to a wave number side lower than 520 cm^{-1}. The diffraction peaks of (111) and (220) which are thought to be contributed to a silicon crystalline lattice are observed by X-ray diffraction. SAS contains hydrogen or halogen of at least 1 atomic percent or more to compensate dangling bonds. SAS is formed by glow discharge decomposition (plasma CVD) of a material gas. As the material gas, Si_2H_6, SiH_2Cl_2, $SiHCl_3$, $SiCl_4$, SiF_4, or the like as well as SiH_4 can be used. Alternatively, GeF_4 may be mixed. The material gas may be diluted with H_2, or H_2 and one or more kinds of rare gas elements selected from He, Ar, Kr, and Ne. A dilution ratio is in the range of 2 to 1000 times. Pressure is in the range of approximately 0.1 to 133 Pa, and a power supply frequency is 1 to 120 MHz, preferably 13 to 60 MHz. A substrate heating temperature may be 300° C. or lower. A concentration of impurities in atmospheric components such as oxygen, nitrogen, and carbon is preferably 1×10^{20} cm^{-1} or less as impurity elements in the film. In particular, an oxygen concentration is $5\times10^{19}/cm^3$ or less, preferably $1\times10^{19}/cm^3$ or less. Here, an amorphous semiconductor layer is formed using a material containing silicon (Si) as its main component (e.g., Si_xGe_{1-x}) by a known method (such as a sputtering method, an LPCVD method, or a plasma CVD method). Then, the amorphous semiconductor layer is crystallized by a known crystallization method such as a laser crystallization method, a thermal crystallization method using RTA or an annealing furnace, or a thermal crystallization method using a metal element which promotes crystallization.

An insulating film **110116** can have a single-layer structure or a stacked-layer structure of an insulating film containing oxygen or nitrogen, such as silicon oxide (SiO_x), silicon nitride (SiN_x), silicon oxynitride (SiO_xN_y) (x>y), or silicon nitride oxide (SiN_xO_y) (x>y).

A gate electrode **110117** can have a single-layer structure of a conductive film or a stacked-layer structure of two or three conductive films. As a material for the gate electrode **110117**, a known conductive film can be used. For example, a single film of an element such as tantalum (Ta), titanium (Ti), molybdenum (Mo), tungsten (W), chromium (Cr), or silicon (Si); a nitride film containing the aforementioned element (typically, a tantalum nitride film, a tungsten nitride film, or a titanium nitride film); an alloy film in which the aforementioned elements are combined (typically, a Mo—W alloy or a Mo—Ta alloy); a silicide film containing the aforementioned element (typically, a tungsten silicide film or a titanium silicide film); and the like can be used. Note that the aforementioned single film, nitride film, alloy film, silicide film, and the like can have a single-layer structure or a stacked-layer structure.

An insulating film **110118** can have a single-layer structure or a stacked-layer structure of an insulating film containing oxygen or nitrogen, such as silicon oxide (SiO_x), silicon nitride (SiN_x), silicon oxynitride (SiO_xN_y) (x>y), or silicon nitride oxide (SiN_xO_y) (x>y); or a film containing carbon, such as a DLC (diamond-like carbon), by a known method (such as a sputtering method or a plasma CVD method).

An insulating film **110119** can have a single-layer structure or a stacked-layer structure of a siloxane resin; an insulating film containing oxygen or nitrogen, such as silicon oxide (SiO_x), silicon nitride (SiN_x), silicon oxynitride (SiO_xN_y) (x>y), or silicon nitride oxide (SiN_xO_y) (x>y); a film containing carbon, such as a DLC (diamond-like carbon); or an organic material such as epoxy, polyimide, polyamide, polyvinyl phenol, benzocyclobutene, or acrylic. Note that a siloxane resin corresponds to a resin having Si—O—Si bonds. Siloxane includes a skeleton structure of a bond of silicon (Si) and oxygen (O). As a substituent, an organic group containing at least hydrogen (such as an alkyl group or aromatic hydrocarbon) is used. Alternatively, a fluoro group, or a fluoro group and an organic group containing at least hydrogen can be used as a substituent. Note that in a display device applicable to the present invention, the insulating film **110119** can be directly provided so as to cover the gate electrode **110117** without provision of the insulating film **110118**.

As a conductive film **110123**, a single film of an element such as Al, Ni, C, W, Mo, Ti, Pt, Cu, Ta, Au, or Mn, a nitride film containing the aforementioned element, an alloy film in which the aforementioned elements are combined, a silicide film containing the aforementioned element, or the like can be used. For example, as an alloy containing a plurality of the aforementioned elements, an Al alloy containing C and Ti, an Al alloy containing Ni, an Al alloy containing C and Ni, an Al alloy containing C and Mn, or the like can be used. Further, when the conductive film has a stacked-layer structure, Al can be interposed between Mo, Ti, or the like; thus, resistance of Al to heat and chemical reaction can be improved.

Next, with reference to the cross-sectional view of the plurality of transistors each having a different structure shown in FIG. **56**A, characteristics of each structure are described.

A transistor **110101** is a single drain transistor. Since the single drain transistor can be formed by a simple method, it is advantageous in low manufacturing cost and high yield. Here, the semiconductor layers **110113** and **110115** have different concentrations of impurities, and the semiconductor layer **110113** is used as a channel formation region and the semiconductor layers **110115** are used as a source region and a drain region. By controlling the concentration of impurities in this manner, resistivity of the semiconductor layer can be controlled. Further, an electrical connection state of the semiconductor layer and the conductive film **110123** can be closer to ohmic contact. Note that as a method of separately forming the semiconductor layers each having different amount of impurities, a method can be used in which impurities are doped in a semiconductor layer using the gate electrode **110117** as a mask.

A transistor **110102** is a transistor in which the gate electrode **110117** is tapered at an angle of at least certain degrees.

Since the transistor can be formed by a simple method, it is advantageous in low manufacturing cost and high yield. Here, the semiconductor layers **110113**, **110114**, and **110115** have different concentrations of impurities. The semiconductor layer **110113** is used as a channel formation region, the semiconductor layers **110114** as lightly doped drain (LDD) regions, and the semiconductor layers **110115** as a source region and a drain region. By controlling the amount of impurities in this manner, resistivity of the semiconductor layer can be controlled. Further, an electrical connection state of the semiconductor layer and the conductive film **110123** can be closer to ohmic contact. Moreover, since the transistor includes the LDD regions, a high electric field is hardly applied inside the transistor, so that deterioration of the element due to hot carriers can be suppressed. Note that as a method of separately forming the semiconductor layers having different amount of impurities, a method can be used in which impurities are doped in a semiconductor layer using the gate electrode **110117** as a mask. In the transistor **110102**, since the gate electrode **110117** is tapered at an angle of at least certain degrees, gradient of the concentration of impurities doped in the semiconductor layer through the gate electrode **110117** can be provided, and the LDD region can be easily formed.

A transistor **110103** is a transistor in which the gate electrode **110117** is formed of at least two layers and a lower gate electrode is longer than an upper gate electrode. In this specification, a shape of the lower and upper gate electrodes is called a hat shape. When the gate electrode **110117** has a hat shape, an LDD region can be formed without addition of a photomask. Note that a structure where the LDD region overlaps with the gate electrode **110117**, like the transistor **110103**, is particularly called a GOLD (gate overlapped LDD) structure. As a method of forming the gate electrode **110117** with a hat shape, the following method may be used.

First, when the gate electrode **110117** is patterned, the lower and upper gate electrodes are etched by dry etching so that side surfaces thereof are inclined (tapered). Then, the inclination of the upper gate electrode is processed to be almost perpendicular by anisotropic etching. Thus, the gate electrode a cross section of which is a hat shape is formed. After that, impurity elements are doped twice, so that the semiconductor layer **110113** used as the channel formation region, the semiconductor layers **110114** used as the LDD regions, and the semiconductor layers **110115** used as a source electrode and a drain electrode are formed.

Note that here, part of the LDD region, which overlaps with the gate electrode **110117**, is referred to as an Lov region, and part of the LDD region, which does not overlap with the gate electrode **110117**, is referred to as an Loff region. The Loff region is highly effective in suppressing an off-current value, whereas it is not very effective in preventing deterioration in an on-current value due to hot carriers by relieving an electric field in the vicinity of the drain. On the other hand, the Lov region is effective in preventing deterioration in the on-current value by relieving the electric field in the vicinity of the drain, whereas it is not very effective in suppressing the off-current value. Thus, it is preferable to form a transistor having a structure appropriate for characteristics of each of the various circuits. For example, a transistor having an Loff region is preferably used as a pixel transistor in order to suppress the off-current value. On the other hand, as a transistor in a peripheral circuit, a transistor having an Lov region is preferably used in order to prevent deterioration in the on-current value by relieving the electric field in the vicinity of the drain.

A transistor **110104** is a transistor including a sidewall **110121** in contact with the side surface of the gate electrode **110117**. When the transistor includes the sidewall **110121**, a region overlapping with the sidewall **110121** can be made to be an LDD region.

A transistor **110105** is a transistor in which an LDD (Loff) region is formed by performing doping of the semiconductor layer with the use of a mask. Thus, the LDD region can surely be formed, and an off-current value of the transistor can be reduced.

A transistor **110106** is a transistor in which an LDD (Lov) region is formed by performing doping of the semiconductor layer with the use of a mask. Thus, the LDD region can surely be formed, and deterioration in an on-current value can be prevented by relieving the electric field in the vicinity of the drain of the transistor.

Next, an example of a method for manufacturing a transistor included in the display device to which the present invention can be applied is described with reference to FIGS. **56**B to **56**G.

Note that a structure and a manufacturing method of a transistor included in the display device to which the present invention can be applied are not limited to those in FIGS. **56**A to **56**G, and various structures and manufacturing methods can be used.

In this embodiment mode, a surface of the substrate **110111**, a surface of the insulating film **110112**, a surface of the semiconductor layer **110113**, a surface of the semiconductor layer **110114**, a surface of the semiconductor layer **110115**, a surface of the insulating film **110116**, a surface of the insulating film **110118**, or a surface of the insulating film **110119** is oxidized or nitrided by using plasma treatment, so that the semiconductor layer or the insulating film can be oxidized or nitrided. By oxidizing or nitriding the semiconductor layer or the insulating film by plasma treatment in such a manner, the surface of the semiconductor layer or the insulating film is modified, and the insulating film can be formed to be denser than an insulating film formed by a CVD method or a sputtering method. Thus, a defect such as a pinhole can be suppressed, and characteristics and the like of the display device can be improved.

First, the surface of the substrate **110111** is washed using hydrofluoric acid (HF), alkaline, or pure water. The substrate **110111** can be a glass substrate using barium borosilicate glass, aluminoborosilicate glass, or the like, a quartz substrate, a ceramic substrate, a metal substrate containing stainless steel, or the like. Further, a substrate formed of plastics typified by polyethylene terephthalate (PET), polyethylene naphthalate (PEN), or polyethersulfone (PES), or a substrate formed of a flexible synthetic resin such as acrylic can also be used. Here, the case where a glass substrate is used as the substrate **110111** is shown.

Here, an oxide film or a nitride film may be formed on the surface of the substrate **110111** by oxidizing or nitriding the surface of the substrate **110111** by plasma treatment (FIG. **56**B). Hereinafter, an insulating film such as an oxide film or a nitride film formed by performing plasma treatment on the surface is also referred to as a plasma-treated insulating film. In FIG. **56**B, an insulating film **110131** is a plasma-treated insulating film. In general, when a semiconductor element such as a thin film transistor is provided over a substrate formed of glass, plastic, or the like, an impurity element such as alkali metal (e.g., Na) or alkaline earth metal included in glass, plastic, or the like might be mixed into the semiconductor element so that the semiconductor element is contaminated; thus, characteristics of the semiconductor element may be adversely affected in some cases. Nitridation of a surface of the substrate formed of glass, plastic, or the like can prevent an impurity element such as alkali metal (e.g., Na) or alkaline earth metal included in the substrate from being mixed into the semiconductor element.

When the surface is oxidized by plasma treatment, the plasma treatment is performed in an oxygen atmosphere (e.g., in an atmosphere of oxygen (O_2) and a rare gas (containing at least one of He, Ne, Ar, Kr, and Xe), in an atmosphere of oxygen, hydrogen (H_2), and a rare gas, or in an atmosphere of dinitrogen monoxide and a rare gas). On the other hand, when the surface is nitrided by plasma treatment, the plasma treatment is performed in a nitrogen atmosphere (e.g., in an atmosphere of nitrogen (N_2) and a rare gas (containing at least one of He, Ne, Ar, Kr, and Xe), in an atmosphere of nitrogen, hydrogen, and a rare gas, or in an atmosphere of NH_3 and a rare gas). As a rare gas, Ar can be used, for example. Alternatively, a gas in which Ar and Kr are mixed may be used. Accordingly, the plasma-treated insulating film contains a rare gas (containing at least one of He, Ne, Ar, Kr, and Xe) used for the plasma treatment. For example, the plasma-treated insulating film contains Ar when Ar is used.

In addition, it is preferable to perform plasma treatment in the atmosphere containing the aforementioned gas, with conditions of an electron density in the range of 1×10^{11} to 1×10^{13} cm^{-3} and a plasma electron temperature in the range of 0.5 to 1.5 eV. Since the plasma electron density is high and the electron temperature in the vicinity of an object to be treated is low, damage by plasma to the object to be treated can be prevented. Further, since the plasma electron density is as high as 1×10^{11} cm^{-3} or more, an oxide film or a nitride film formed by oxidizing or nitriding the object to be treated by plasma treatment is superior in its uniformity of thickness and the like as well as being dense, as compared with a film formed by a CVD method, a sputtering method, or the like. Alternatively, since the plasma electron temperature is as low as 1 eV or less, oxidation or nitridation can be performed at a lower temperature as compared with a conventional plasma treatment or thermal oxidation. For example, oxidation or nitridation can be performed sufficiently even when plasma treatment is performed at a temperature lower than a strain point of a glass substrate by 100 degrees or more. Note that as frequency for generating plasma, high frequency waves such as microwaves (2.45 GHz) can be used. Note that hereinafter, plasma treatment is performed using the aforementioned conditions unless otherwise specified.

Note that although FIG. **56**B shows the case where the plasma-treated insulating film is formed by plasma treatment on the surface of the substrate **110111**, this embodiment mode includes the case where a plasma-treated insulating film is not formed on the surface of the substrate **110111**.

Note that although a plasma-treated insulating film formed by plasma treatment on the surface of the object to be treated is not shown in FIGS. **56**C to **56**G, this embodiment mode includes the case where a plasma-treated insulating film formed by plasma treatment exists on the surface of the substrate **110111**, the insulating film **110112**, the semiconductor layer **110113**, the semiconductor layer **110114**, the semiconductor layer **110115**, the insulating film **110116**, the insulating film **110118**, or the insulating film **110119**.

Next, the insulating film **110112** is formed over the substrate **110111** by a known method (such as a sputtering method, an LPCVD method, or a plasma CVD method) (FIG. **56**C). For the insulating film **110112**, silicon oxide (SiO_x) or silicon oxynitride (SiO_xN_y) (x>y) can be used.

Here, a plasma-treated insulating film may be formed on the surface of the insulating film **110112** by oxidizing or nitriding the surface of the insulating film **110112** by plasma treatment. By oxidizing the surface of the insulating film **110112**, the surface of the insulating film **110112** is modified, and a dense film with fewer defects such as a pinhole can be obtained. Further, by oxidizing the surface of the insulating film **110112**, the plasma-treated insulating film containing a little amount of N atoms can be formed; thus, interface characteristics of the plasma-treated insulating film and a semiconductor layer are improved when the semiconductor layer is provided over the plasma-treated insulating film. The plasma-treated insulating film contains a rare gas (containing at least one of He, Ne, Ar, Kr, and Xe) used for the plasma treatment. Note that the plasma treatment can be similarly performed under the aforementioned conditions.

Next, the island-shaped semiconductor layers **110113** and **110114** are formed over the insulating film **110112** (FIG. **56**D). The island-shaped semiconductor layers **110113** and **110114** can be formed in such a manner that an amorphous semiconductor layer is formed over the insulating film **110112** by using a material containing silicon (Si) as its main component (e.g., Si_xGe_{1-x}) or the like by a known method (such as a sputtering method, an LPCVD method, or a plasma CVD method), the amorphous semiconductor layer is crystallized, and the semiconductor layer is selectively etched. Note that crystallization of the amorphous semiconductor layer can be performed by a known crystallization method such as a laser crystallization method, a thermal crystallization method using RTA or an annealing furnace, a thermal crystallization method using a metal element which promotes crystallization, or a method in which these methods are combined. Here, end portions of the island-shaped semiconductor layers are provided with an angle of about 90° (θ=85 to 100°). Alternatively, the semiconductor layer **110114** to be a low concentration drain region may be formed by doping impurities with the use of a mask.

Here, a plasma-treated insulating film may be formed on the surfaces of the semiconductor layers **110113** and **110114** by oxidizing or nitriding the surfaces of the semiconductor layers **110113** and **110114** by plasma treatment. For example, when Si is used for the semiconductor layers **110113** and **110114**, silicon oxide (SiO_x) or silicon nitride (SiN_x) is formed as the plasma-treated insulating film. Alternatively, after being oxidized by plasma treatment, the semiconductor layers **110113** and **110114** may be nitrided by performing plasma treatment again. In this case, silicon oxide (SiO_x) is formed in contact with the semiconductor layers **110113** and **110114**, and silicon nitride oxide (SiN_xO_y) (x>y) is formed on the surface of the silicon oxide. Note that when the semiconductor layer is oxidized by plasma treatment, the plasma treatment is performed in an oxygen atmosphere (e.g., in an atmosphere of oxygen (O_2) and a rare gas (containing at least one of He, Ne, Ar, Kr, and Xe), in an atmosphere of oxygen, hydrogen (H_2), and a rare gas, or in an atmosphere of dinitrogen monoxide and a rare gas). On the other hand, when the semiconductor layer is nitrided by plasma treatment, the plasma treatment is performed in a nitrogen atmosphere (e.g., in an atmosphere of nitrogen (N_2) and a rare gas (containing at least one of He, Ne, Ar, Kr, and Xe), in an atmosphere of nitrogen, hydrogen, and a rare gas, or in an atmosphere of NH_3 and a rare gas). As a rare gas, Ar can be used, for example. Alternatively, a gas in which Ar and Kr are mixed may be used. Accordingly, the plasma-treated insulating film contains a rare gas (containing at least one of He, Ne, Ar, Kr, and Xe) used for the plasma treatment. For example, the plasma-treated insulating film contains Ar when Ar is used.

Next, the insulating film **110116** is formed (FIG. **56**E). The insulating film **110116** can have a single-layer structure or a stacked-layer structure of an insulating film containing oxygen or nitrogen, such as silicon oxide (SiO_x), silicon nitride (SiN_x), silicon oxynitride (SiO_xN_y) (x>y), or silicon nitride oxide (SiN_xO_y) (x>y), by a known method (such as a sputtering method, an LPCVD method, or a plasma CVD method). Note that when the plasma-treated insulating film is formed on the surfaces of the semiconductor layers **110113** and **110114** by performing plasma treatment on the surfaces of the semiconductor layers **110113** and **110114**, the plasma-treated insulating film can be used as the insulating film **110116**.

Here, the surface of the insulating film **110116** may be oxidized or nitrided by plasma treatment, so that a plasma-treated insulating film is formed on the surface of the insulating film **110116**. Note that the plasma-treated insulating film contains a rare gas (containing at least one of He, Ne, Ar, Kr, and Xe) used for the plasma treatment. The plasma treatment can be similarly performed under the aforementioned conditions.

Alternatively, after the insulating film **110116** is oxidized by performing plasma treatment once in an oxygen atmosphere, the insulating film **110116** may be nitrided by performing plasma treatment again in a nitrogen atmosphere. By oxidizing or nitriding the surface of the insulating film **110116** by plasma treatment in such a manner, the surface of the insulating film **110116** is modified, and a dense film can be formed. An insulating film obtained by plasma treatment is denser and has fewer defects such as a pinhole, as compared with an insulating film formed by a CVD method, a sputtering method, or the like. Thus, characteristics of a thin film transistor can be improved.

Next, the gate electrode **110117** is formed (FIG. **56**F). The gate electrode **110117** can be formed by a known method (such as a sputtering method, an LPCVD method, or a plasma CVD method).

In the transistor **110101**, the semiconductor layers **110115** used as the source region and the drain region can be formed by doping impurities after the gate electrode **110117** is formed.

In the transistor **110102**, the semiconductor layers **110114** used as the LDD regions and the semiconductor layers **110115** used as the source region and the drain region can be formed by doping impurities after the gate electrode **110117** is formed.

In the transistor **110103**, the semiconductor layers **110114** used as the LDD regions and the semiconductor layers **110115** used as the source region and the drain region can be formed by doping impurities after the gate electrode **110117** is formed.

In the transistor **110104**, the semiconductor layers **110114** used as the LDD regions and the semiconductor layers **110115** used as the source region and the drain region can be formed by doping impurities after the sidewall **110121** is formed on the side surface of the gate electrode **110117**.

Note that silicon oxide (SiO_x) or silicon nitride (SiN_x) can be used for the sidewall **110121**. As a method of forming the sidewall **110121** on the side surface of the gate electrode **110117**, a method can be used, for example, in which a silicon oxide (SiO_x) film or a silicon nitride (SiN_x) film is formed by a known method after the gate electrode **110117** is formed, and then, the silicon oxide (SiO_x) film or the silicon nitride (SiN_x) film is etched by anisotropic etching. Thus, the silicon oxide (SiO_x) film or the silicon nitride (SiN_x) film remains only on the side surface of the gate electrode **110117**, so that the sidewall **110121** can be formed on the side surface of the gate electrode **110117**.

In the transistor **110105**, the semiconductor layers **110114** used as the LDD (Loft) regions and the semiconductor layer **110115** used as the source region and the drain region can be formed by doping impurities after a mask **110122** is formed to cover the gate electrode **110117**.

In the transistor **110106**, the semiconductor layers **110114** used as the LDD (Lov) regions and the semiconductor layers **110115** used as the source region and the drain region can be formed by doping impurities after the gate electrode **110117** is formed.

Next, the insulating film **110118** is formed (FIG. **56**G). The insulating film **110118** can have a single-layer structure or a stacked-layer structure of an insulating film containing oxygen or nitrogen, such as silicon oxide (SiO_x), silicon nitride (SiN_x), silicon oxynitride (SiO_xN_y) (x>y), or silicon nitride oxide (SiN_xO_y) (x>y); or a film containing carbon, such as a DLC (diamond-like carbon), by a known method (such as a sputtering method or a plasma CVD method).

Here, the surface of the insulating film **110118** may be oxidized or nitrided by plasma treatment, so that a plasma-treated insulating film is formed on the surface of the insulating film **110118**. Note that the plasma-treated insulating film contains a rare gas (containing at least one of He, Ne, Ar, Kr, and Xe) used for the plasma treatment. The plasma treatment can be similarly performed under the aforementioned conditions.

Next, the insulating film **110119** is formed. The insulating film **110119** can have a single-layer structure or a stacked-layer structure of an organic material such as epoxy, polyimide, polyamide, polyvinyl phenol, benzocyclobutene, or acrylic; or a siloxane resin, in addition to an insulating film containing oxygen or nitrogen, such as silicon oxide (SiO_x), silicon nitride (SiN_x), silicon oxynitride (SiO_xN_y) (x>y), or silicon nitride oxide (SiN_xO_y) (x>y); or a film containing carbon, such as a DLC (diamond-like carbon), by known method (such as a sputtering method or a plasma CVD method). Note that a siloxane resin corresponds to a resin having Si—O—Si bonds. Siloxane includes a skeleton structure of a bond of silicon (Si) and oxygen (O). As a substituent, an organic group containing at least hydrogen (such as an alkyl group or aromatic hydrocarbon) is used. Alternatively, a fluoro group, or a fluoro group and an organic group containing at least hydrogen can be used as a substituent. In addition, the plasma-treated insulating film contains a rare gas (containing at least one of He, Ne, Ar, Kr, and Xe) used for the plasma treatment. For example, the plasma-treated insulating film contains Ar when Ar is used.

When an organic material such as polyimide, polyamide, polyvinyl phenol, benzocyclobutene, or acrylic, or a siloxane resin is used for the insulating film **110119**, the surface of the insulating film **110119** can be modified by oxidizing or nitriding the surface of the insulating film by plasma treatment. Modification of the surface improves strength of the insulating film **110119**, and physical damage such as a crack generated when an opening is formed, for example, or film reduction in etching can be reduced. Further, when the conductive film **110123** is formed over the insulating film **110119**, modification of the surface of the insulating film **110119** improves adhesion to the conductive film. For example, when a siloxane resin is used for the insulating film **110119** and nitrided by plasma treatment, a plasma-treated insulating film containing nitrogen or a rare gas is formed by nitriding a surface of the siloxane resin, and physical strength is improved.

Next, a contact hole is formed in the insulating films **110119**, **110118**, and **110116** in order to form the conductive film **110123** which is electrically connected to the semiconductor layer **110115**. Note that the contact hole may have a tapered shape. Thus, coverage with the conductive film **110123** can be improved.

FIG. **60** shows cross-sectional structures of a bottom-gate transistor and a capacitor.

A first insulating film (an insulating film **110502**) is formed over an entire surface of a substrate **110501**. The first insulating film can prevent impurities from the substrate from adversely affecting a semiconductor layer and changing properties of a transistor. That is, the first insulating film functions as a base film. Thus, a transistor with high reliability can be formed. As the first insulating film, a single layer or a stacked layer of a silicon oxide film, a silicon nitride film, a silicon oxynitride film (SiO_xN_y), or the like can be used.

A first conductive layer (conductive layers **110503** and **110504**) is formed over the first insulating film. The conductive layer **110503** includes a portion functioning as a gate electrode of a transistor **110520**. The conductive layer **110504** includes a portion functioning as a first electrode of a capacitor **110521**. As the first conductive layer, an element such as Ti, Mo, Ta, Cr, W, Al, Nd, Cu, Ag, Au, Pt, Nb, Si, Zn, Fe, Ba, or Ge, or an alloy of these elements can be used. Alternatively, a stacked layer of these elements (including the alloy thereof) can be used.

A second insulating film (an insulating film **110522**) is formed to cover at least the first conductive layer. The second insulating film functions as a gate insulating film. As the second insulating film, a single layer or a stacked layer of a silicon oxide film, a silicon nitride film, a silicon oxynitride film (SiO_xN_y), or the like can be used.

Note that for a portion of the second insulating film, which is in contact with the semiconductor layer, a silicon oxide film is preferably used. This is because the trap level at the interface between the semiconductor layer and the second insulating film is lowered.

When the second insulating film is in contact with Mo, a silicon oxide film is preferably used for a portion of the second insulating film in contact with Mo. This is because the silicon oxide film does not oxidize Mo.

A semiconductor layer is formed in part of a portion over the second insulating film, which overlaps with the first conductive layer, by a photolithography method, an inkjet method, a printing method, or the like. Part of the semiconductor layer extends to a portion over the second insulating film, which does not overlap with the first conductive layer. The semiconductor layer includes a channel formation region (a channel formation region **110510**), an LDD region (LDD regions **110508** and **110509**), and an impurity region (impurity regions **110505**, **110506**, and **110507**). The channel formation region **110510** functions as a channel formation region of the transistor **110520**. The LDD regions **110508** and **110509** function as LDD regions of the transistor **110520**. Note that the LDD regions **110508** and **110509** are not necessarily formed. The impurity region **110505** includes a portion functioning as one of a source electrode and a drain electrode of the transistor **110520**. The impurity region **110506** includes a portion functioning as the other of the source electrode and the drain electrode of the transistor **110520**. The impurity region **110507** includes a portion functioning as a second electrode of the capacitor **110521**.

A third insulating film (an insulating film **110511**) is entirely formed. A contact hole is selectively formed in part of the third insulating film. The insulating film **110511** functions as an interlayer film. As the third insulating film, an inorganic material (e.g., silicon oxide, silicon nitride, or silicon oxynitride), an organic compound material having a low dielectric constant (e.g., a photosensitive or nonphotosensitive organic resin material), or the like can be used. Alternatively, a material containing siloxane may be used. Note that siloxane is a material in which a skeleton structure is formed by a bond of silicon (Si) and oxygen (O). As a substitute, an organic group containing at least hydrogen (such as an alkyl group or aromatic hydrocarbon) is used. Alternatively, a fluoro group, or a fluoro group and an organic group containing at least hydrogen may be used as a substituent.

A second conductive layer (conductive layers **110512** and **110513**) is formed over the third insulating film. The conductive layer **110512** is connected to the other of the source electrode and the drain electrode of the transistor **110520** through the contact hole formed in the third insulating film. Thus, the conductive layer **110512** includes a portion functioning as the other of the source electrode and the drain electrode of the transistor **110520**. The conductive layer **110513** includes a portion functioning as the first electrode of the capacitor **110521**. As the second conductive layer, an element such as Ti, Mo, Ta, Cr, W, Al, Nd, Cu, Ag, Au, Pt, Nb, Si, Zn, Fe, Ba, or Ge, or an alloy of these elements can be used. Alternatively, a stacked layer of these elements (including the alloy thereof) can be used.

Note that in steps after forming the second conductive layer, various insulating films or various conductive films may be formed.

Next, structures of a transistor and a capacitor are described in the case where an amorphous silicon (a-Si:H) film is used as a semiconductor layer of the transistor.

FIG. **57** shows cross-sectional structures of a top-gate transistor and a capacitor.

A first insulating film (an insulating film **110202**) is formed over an entire surface of a substrate **110201**. The first insulating film can prevent impurities from the substrate from adversely affecting a semiconductor layer and changing properties of a transistor. That is, the first insulating film functions as a base film. Thus, a transistor with high reliability can be formed. As the first insulating film, a single layer or a stacked layer of a silicon oxide film, a silicon nitride film, a silicon oxynitride film (SiO_xN_y), or the like can be used.

Note that the first insulating film is not necessarily formed. When the first insulating film is not formed, reduction in the number of steps and reduction in manufacturing cost can be realized. Further, since the structure can be simplified, the yield can be improved.

A first conductive layer (conductive layers **110203**, **110204**, and **110205**) is formed over the first insulating film. The conductive layer **110203** includes a portion functioning as one of a source electrode and a drain electrode of a transistor **110220**. The conductive layer **110204** includes a portion functioning as the other of the source electrode and the drain electrode of the transistor **110220**. The conductive layer **110205** includes a portion functioning as a first electrode of a capacitor **110221**. As the first conductive layer, an element such as Ti, Mo, Ta, Cr, W, Al, Nd, Cu, Ag, Au, Pt, Nb, Si, Zn, Fe, Ba, or Ge, or an alloy of these elements can be used. Alternatively, a stacked layer of these elements (including the alloy thereof) can be used.

A first semiconductor layer (semiconductor layers **110206** and **110207**) is formed above the conductive layers **110203** and **110204**. The semiconductor layer **110206** includes a portion functioning as one of the source electrode and the drain electrode. The semiconductor layer **110207** includes a portion functioning as the other of the source electrode and the drain electrode. As the first semiconductor layer, silicon containing phosphorus or the like can be used, for example.

A second semiconductor layer (a semiconductor layer **110208**) is formed over the first insulating film and between the conductive layer **110203** and the conductive layer **110204**. Part of the semiconductor layer **110208** extends over the conductive layers **110203** and **110204**. The semiconductor layer **110208** includes a portion functioning as a channel formation region of the transistor **110220**. As the second semiconductor layer, a semiconductor layer having no crystallinity such as an amorphous silicon (a-Si:H) layer, a semiconductor layer such as a microcrystalline semiconductor (μ-Si:H) layer, or the like can be used.

A second insulating film (insulating films **110209** and **110210**) is formed to cover at least the semiconductor layer **110208** and the conductive layer **110205**. The second insulating film functions as a gate insulating film. As the second insulating film, a single layer or a stacked layer of a silicon oxide film, a silicon nitride film, a silicon oxynitride film (SiO_xN_y), or the like can be used.

Note that for a portion of the second insulating film, which is in contact with the second semiconductor layer, a silicon oxide film is preferably used. This is because the trap level at the interface between the second semiconductor layer and the second insulating film is lowered.

When the second insulating film is in contact with Mo, a silicon oxide film is preferably used for a portion of the second insulating film in contact with Mo. This is because the silicon oxide film does not oxidize Mo.

A second conductive layer (conductive layers **110211** and **110212**) is formed over the second insulating film. The conductive layer **110211** includes a portion functioning as a gate electrode of the transistor **110220**. The conductive layer **110212** functions as a second electrode of the capacitor **110221** or a wiring. As the second conductive layer, an element such as Ti, Mo, Ta, Cr, W, Al, Nd, Cu, Ag, Au, Pt, Nb, Si, Zn, Fe, Ba, or Ge, or an alloy of these elements can be used. Alternatively, a stacked layer of these elements (including the alloy thereof) can be used.

Note that in steps after forming the second conductive layer, various insulating films or various conductive films may be formed.

FIG. **58** shows cross-sectional structures of an inversely staggered (bottom gate) transistor and a capacitor. In particular, the transistor shown in FIG. **58** has a channel-etched structure.

A first insulating film (an insulating film **110302**) is formed over an entire surface of a substrate **110301**. The first insulating film can prevent impurities from the substrate from adversely affecting a semiconductor layer and changing properties of a transistor. That is, the first insulating film functions as a base film. Thus, a transistor with high reliability can be formed. As the first insulating film, a single layer or a stacked layer of a silicon oxide film, a silicon nitride film, a silicon oxynitride film (SiO_xN_y), or the like can be used.

Note that the first insulating film is not necessarily formed. When the first insulating film is not formed, reduction in the number of steps and reduction in manufacturing cost can be realized. Further, since the structure can be simplified, the yield can be improved.

A first conductive layer (conductive layers **110303** and **110304**) is formed over the first insulating film. The conductive layer **110303** includes a portion functioning as a gate electrode of a transistor **110320**. The conductive layer **110304** includes a portion functioning as a first electrode of a capacitor **110321**. As the first conductive layer, an element such as Ti, Mo, Ta, Cr, W, Al, Nd, Cu, Ag, Au, Pt, Nb, Si, Zn, Fe, Ba, or Ge, or an alloy of these elements can be used. Alternatively, a stacked layer of these elements (including the alloy thereof) can be used.

A second insulating film (an insulating film **110305**) is formed to cover at least the first conductive layer. The second insulating film functions as a gate insulating film. As the second insulating film, a single layer or a stacked layer of a silicon oxide film, a silicon nitride film, a silicon oxynitride film (SiO_xN_y), or the like can be used.

Note that for a portion of the second insulating film, which is in contact with the semiconductor layer, a silicon oxide film is preferably used. This is because the trap level at the interface between the semiconductor layer and the second insulating film is lowered.

When the second insulating film is in contact with Mo, a silicon oxide film is preferably used for a portion of the second insulating film in contact with Mo. This is because the silicon oxide film does not oxidize Mo.

A first semiconductor layer (a semiconductor layer **110306**) is formed in part of a portion over the second insulating film, which overlaps with the first conductive layer, by a photolithography method, an inkjet method, a printing method, or the like. Part of the semiconductor layer **110306** extends to a portion over the second insulating film, which does not overlap with the first conductive layer. The semiconductor layer **110306** includes a portion functioning as a channel formation region of the transistor **110320**. As the semiconductor layer **110306**, a semiconductor layer having no crystallinity such as an amorphous silicon (a-Si:H) layer, a semiconductor layer such as a microcrystalline semiconductor (μ-Si:H) layer, or the like can be used.

A second semiconductor layer (semiconductor layers **110307** and **110308**) is formed over part of the first semiconductor layer. The semiconductor layer **110307** includes a portion functioning as one of a source electrode and a drain electrode. The semiconductor layer **110308** includes a portion functioning as the other of the source electrode and the drain electrode. As the second semiconductor layer, silicon containing phosphorus or the like can be used, for example.

A second conductive layer (conductive layers **110309**, **110310**, and **110311**) is formed over the second semiconductor layer and the second insulating film. The conductive layer **110309** includes a portion functioning as one of the source electrode and the drain electrode of the transistor **110320**. The conductive layer **110310** includes a portion functioning as the other of the source electrode and the drain electrode of the transistor **110320**. The conductive layer **110311** includes a portion functioning as a second electrode of the capacitor **110321**. As the second conductive layer, an element such as Ti, Mo, Ta, Cr, W, Al, Nd, Cu, Ag, Au, Pt, Nb, Si, Zn, Fe, Ba, or Ge, or an alloy of these elements can be used. Alternatively, a stacked layer of these elements (including the alloy thereof) can be used.

Note that in steps after forming the second conductive layer, various insulating films or various conductive films may be formed.

Here, an example of a step which is characteristic of the channel-etched type transistor is described. The first semiconductor layer and the second semiconductor layer can be formed using the same mask. Specifically, the first semiconductor layer and the second semiconductor layer are continuously formed. Further, the first semiconductor layer and the second semiconductor layer are formed using the same mask.

Another example of a step which is characteristic of the channel-etched type transistor is described. The channel formation region of the transistor can be formed without using an additional mask. Specifically, after the second conductive layer is formed, part of the second semiconductor layer is removed using the second conductive layer as a mask. Alternatively, part of the second semiconductor layer is removed by using the same mask as the second conductive layer. The first semiconductor layer below the removed second semiconductor layer serves as the channel formation region of the transistor.

FIG. **59** shows cross-sectional structures of an inversely staggered (bottom gate) transistor and a capacitor. In particular, the transistor shown in FIG. **59** has a channel protection (channel stop) structure.

A first insulating film (an insulating film **110402**) is formed over an entire surface of a substrate **110401**. The first insulating film can prevent impurities from the substrate from adversely affecting a semiconductor layer and changing properties of a transistor. That is, the first insulating film functions as a base film. Thus, a transistor with high reliability can be formed. As the first insulating film, a single layer or a stacked layer of a silicon oxide film, a silicon nitride film, a silicon oxynitride film (SiO_xN_y), or the like can be used.

Note that the first insulating film is not necessarily formed. When the first insulating film is not formed, reduction in the number of steps and reduction in manufacturing cost can be realized. Further, since the structure can be simplified, the yield can be improved.

A first conductive layer (conductive layers **110403** and **110404**) is formed over the first insulating film. The conductive layer **110403** includes a portion functioning as a gate electrode of a transistor **110420**. The conductive layer **110404** includes a portion functioning as a first electrode of a capacitor **110421**. As the first conductive layer, an element such as Ti, Mo, Ta, Cr, W, Al, Nd, Cu, Ag, Au, Pt, Nb, Si, Zn, Fe, Ba, or Ge, or an alloy of these elements can be used. Alternately, a stacked layer of these elements (including the alloy thereof) can be used.

A second insulating film (an insulating film **110405**) is formed to cover at least the first conductive layer. The second insulating film functions as a gate insulating film. As the second insulating film, a single layer or a stacked layer of a silicon oxide film, a silicon nitride film, a silicon oxynitride film (SiO_xN_y), or the like can be used.

Note that for a portion of the second insulating film, which is in contact with the semiconductor layer, a silicon oxide film is preferably used. This is because the trap level at the interface between the semiconductor layer and the second insulating film is lowered.

When the second insulating film is in contact with Mo, a silicon oxide film is preferably used for a portion of the second insulating film in contact with Mo. This is because the silicon oxide film does not oxidize Mo.

A first semiconductor layer (a semiconductor layer **110406**) is formed in part of a portion over the second insulating film, which overlaps with the first conductive layer, by a photolithography method, an inkjet method, a printing method, or the like. Part of the semiconductor layer **110406** extends to a portion over the second insulating film, which does not overlap with the first conductive layer. The semiconductor layer **110406** includes a portion functioning as a channel formation region of the transistor **110420**. As the semiconductor layer **110406**, a semiconductor layer having no crystallinity such as an amorphous silicon (a-Si:H) layer, a semiconductor layer such as a microcrystalline semiconductor (μ-Si:H) layer, or the like can be used.

A third insulating film (an insulating film **110412**) is formed over part of the first semiconductor layer. The insulating film **110412** prevents the channel formation region of the transistor **110420** from being removed by etching. That is, the insulating film **110412** functions as a channel protection film (a channel stop film) As the third insulating film, a single layer or a stacked layer of a silicon oxide film, a silicon nitride film, a silicon oxynitride film (SiO_xN_y), or the like can be used.

A second semiconductor layer (semiconductor layers **110407** and **110408**) is formed over part of the first semiconductor layer and part of the third insulating film. The semiconductor layer **110407** includes a portion functioning as one of a source electrode and a drain electrode. The semiconductor layer **110408** includes a portion functioning as the other of the source electrode and the drain electrode. As the second semiconductor layer, silicon containing phosphorus or the like can be used, for example.

A second conductive layer (conductive layers **110409**, **110410**, and **110411**) is formed over the second semiconductor layer. The conductive layer **110409** includes a portion functioning as one of the source electrode and the drain electrode of the transistor **110420**. The conductive layer **110410** includes a portion functioning as the other of the source electrode and the drain electrode of the transistor **110420**. The conductive layer **110411** includes a portion functioning as a second electrode of the capacitor **110421**. As the second conductive layer, an element such as Ti, Mo, Ta, Cr, W, Al, Nd, Cu, Ag, Au, Pt, Nb, Si, Zn, Fe, Ba, or Ge, or an alloy of these elements can be used. Alternately, a stacked layer of these elements (including the alloy thereof) can be used.

Note that in steps after forming the second conductive layer, various insulating films or various conductive films may be formed.

Here, an example of a step which is characteristic of the channel protection type transistor is described. The first semiconductor layer, the second semiconductor layer, and the second conductive layer can be formed using the same mask. At the same time, the channel formation region can be formed. Specifically, the first semiconductor layer is formed, and then, the third insulating film (i.e., the channel protection film or the channel stop film) is patterned using a mask. Next, the second semiconductor layer and the second conductive layer are continuously formed. Then, after the second conductive layer is formed, the first semiconductor layer, the second semiconductor layer, and the second conductive film are patterned using the same mask. Note that part of the first semiconductor layer below the third insulating film is protected by the third insulating film, and thus is not removed by etching. This part (a part of the first semiconductor layer over which the third insulating film is formed) serves as the channel formation region.

Note that although this embodiment mode is described with reference to various drawings, the contents (or part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in another drawing. Further, much more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or part of the contents) described in each drawing in this embodiment mode can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in a drawing in another embodiment mode or embodiment. Further, much more drawings can be formed by combining each part in each drawing in this embodiment mode with part of another embodiment mode or embodiment.

Note that this embodiment mode shows examples of embodying, slightly transforming, partially modifying, improving, describing in detail, or applying the contents (or part of the contents) described in other embodiment modes and embodiments, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment mode.

[Embodiment Mode 13]

In this embodiment mode, a structure of an EL element is described. In particular, a structure of an inorganic EL element is described.

An inorganic EL element is classified as either a dispersion type inorganic EL element or a thin-film type inorganic EL element, depending on its element structure. These elements differ in that the former includes an electroluminescent layer in which particles of a light-emitting material are dispersed in a binder, whereas the latter includes an electroluminescent layer formed of a thin film of a light-emitting material. However, the former and the latter have in common in that they need electrons accelerated by a high electric field. Note that mechanisms for obtaining light emission are donor-acceptor recombination light emission which utilizes a donor level and an acceptor level; and localized light emission which utilizes inner-shell electron transition of a metal ion. In general, donor-acceptor recombination light emission is employed in dispersion type inorganic EL elements and localized light emission is employed in thin-film type inorganic EL elements in many cases.

A light-emitting material includes a base material and an impurity element to be a luminescence center. Light emission of various colors can be obtained by changing the impurity element to be included. The light-emitting material can be formed using various methods, such as a solid phase method or a liquid phase method (a coprecipitation method). Further, a liquid phase method such as a spray pyrolysis method, a double decomposition method, a method employing precursor pyrolysis, a reverse micelle method, a method in which one or more of these methods are combined with high-temperature baking, or a freeze-drying method, or the like can be used.

A solid phase method is a method in which a base material and an impurity element or a compound containing an impurity element are weighed, mixed in a mortar, and heated and baked in an electric furnace so as to be reacted; thus, the impurity element is included in the base material. The baking temperature is preferably 700 to 1500° C. This is because a solid-phase reaction does not proceed when the temperature is too low, and the base material decomposes when the temperature is too high. Note that although the materials may be baked in powder form, they are preferably baked in pellet form. Although a solid phase method needs a comparatively high temperature, it is a simple method, and thus has high productivity and is suitable for mass production.

A liquid phase method (a coprecipitation method) is a method in which a base material or a compound containing a base material, and an impurity element or a compound containing an impurity element are reacted in a solution, dried, and then baked. Particles of a light-emitting material are uniformly distributed, and the reaction can progress even when the particles are small and the baking temperature is low.

As a base material to be used for a light-emitting material, sulfide, oxide, or nitride can be used. As sulfide, zinc sulfide (ZnS), cadmium sulfide (CdS), calcium sulfide (CaS), yttrium sulfide (Y_2S_3), gallium sulfide (Ga_2S_3), strontium sulfide (SrS), barium sulfide (BaS), or the like can be used, for example. As oxide, zinc oxide (ZnO), yttrium oxide (Y_2O_3), or the like can be used, for example. As nitride, aluminum nitride (AlN), gallium nitride (GaN), indium nitride (InN), or the like can be used, for example. Further, zinc selenide (ZnSe), zinc telluride (ZnTe), or the like; or a ternary mixed crystal such as calcium gallium sulfide ($CaGa_2S_4$), strontium gallium sulfide ($SrGa_2S_4$), or barium gallium sulfide ($BaGa_2S_4$) may be used.

As a luminescence center for localized light emission, manganese (Mn), copper (Cu), samarium (Sm), terbium (Tb), erbium (Er), thulium (Tm), europium (Eu), cerium (Ce), praseodymium (Pr), or the like can be used. Note that a halogen element such as fluorine (F) or chlorine (Cl) may be added for charge compensation.

On the other hand, as a luminescence center for donor-acceptor recombination light emission, a light-emitting material including a first impurity element forming a donor level and a second impurity element forming an acceptor level can be used. As the first impurity element, fluorine (F), chlorine (Cl), aluminum (Al), or the like can be used, for example. As the second impurity element, copper (Cu), silver (Ag), or the like can be used, for example.

When the light-emitting material for donor-acceptor recombination light emission is synthesized by a solid phase method, a base material, the first impurity element or a compound containing the first impurity element, and the second impurity element or a compound containing the second impurity element are weighed, mixed in a mortar, and heated and baked in an electric furnace. As the base material, the aforementioned base material can be used. As the first impurity element or the compound containing the first impurity element, fluorine (F), chlorine (Cl), aluminum sulfide (Al_2S_3), or the like can be used, for example. As the second impurity element or the compound containing the second impurity element, copper (Cu), silver (Ag), copper sulfide (Cu_2S), silver sulfide (Ag_2S), or the like can be used, for example. The baking temperature is preferably 700 to 1500° C. This is because a solid-phase reaction does not proceed when the temperature is too low, and the base material decomposes when the temperature is too high. Note that although the materials may be baked in powder form, they are preferably baked in pellet form.

As the impurity element in the case of using a solid phase reaction, compounds including the first impurity element and the second impurity element may be used in combination. In this case, the impurity elements are easily diffused, and the solid phase reaction proceeds readily, so that a uniform light-emitting material can be obtained. Further, since an unnecessary impurity element is not included, a light-emitting material with high purity can be obtained. As the compound including the first impurity element and the second impurity element, copper chloride (CuCl), silver chloride (AgCl), or the like can be used, for example.

Note that the concentration of these impurity elements is in the range of 0.01 to 10 atomic percent, and is preferably in the range of 0.05 to 5 atomic percent with respect to the base material.

In the case of a thin-film type inorganic EL element, an electroluminescent layer includes the aforementioned light-emitting material, and can be formed using a physical vapor deposition (PVD) method such as a sputtering method or a vacuum evaporation method, for example, a resistance heating evaporation method or an electron beam evaporation (EB evaporation) method, a chemical vapor deposition (CVD) method such as a metal organic CVD method or a low-pressure hydride transport CVD method, an atomic layer epitaxy (ALE) method, or the like.

FIGS. **61**A to **61**C each show an example of a thin-film type inorganic EL element which can be used as the light-emitting element. In FIGS. **61**A to **61**C, a light-emitting element includes a first electrode layer **120100**, an electroluminescent layer **120102**, and a second electrode layer **120103**.

The light-emitting elements shown in FIGS. **61**B and **61**C each have a structure where an insulating film is provided between the electrode layer and the electroluminescent layer in the light-emitting element in FIG. **61**A. The light-emitting element shown in FIG. **61**B includes an insulating film **120104** between the first electrode layer **120100** and the electroluminescent layer **120102**. The light-emitting element shown in FIG. **61**C includes an insulating film **120105** between the first electrode layer **120100** and the electroluminescent layer **120102**, and an insulating film **120106** between the second electrode layer **120103** and the electroluminescent layer **120102**.

In such a manner, the insulating film may be provided between the electroluminescent layer and one of the electrode layers interposing the electroluminescent layer, or may be provided between the electroluminescent layer and each of the electrode layers interposing the electroluminescent layer. The insulating film may be a single layer or stacked layers including a plurality of layers.

Note that the insulating film **120104** is provided in contact with the first electrode layer **120100** in FIG. **61**B; however, the insulating film **120104** may be provided in contact with the second electrode layer **120103** by reversing the order of the insulating film and the electroluminescent layer.

In the case of a dispersion type inorganic EL, a film-shaped electroluminescent layer is formed by dispersing particulate light-emitting materials in a binder. When particles with a desired size cannot be sufficiently obtained by a method of forming the light-emitting material, the light-emitting materials may be processed into particles by being crushed in a mortar or the like. The binder is a substance for fixing the particulate light-emitting material in a dispersed state and maintaining the shape as the electroluminescent layer. The light-emitting material is uniformly dispersed in the electroluminescent layer and fixed by the binder.

In the case of a dispersion type inorganic EL, as a method of forming the electroluminescent layer, a droplet discharging method by which the electroluminescent layer can be selectively formed, a printing method (such as screen printing or offset printing), a coating method such as a spin coating method, a dipping method, a dispenser method, or the like can be used. The thickness of the electroluminescent layer is not particularly limited, but preferably in the range of 10 to 1000 nm. In the electroluminescent layer including the light-emitting material and the binder, a ratio of the light-emitting material is preferably 50 wt % or more and 80 wt % or less.

FIGS. **62**A to **62**C each show an example of a dispersion type inorganic EL element which can be used as the light-emitting element. A light-emitting element in FIG. **62**A has a stacked-layer structure of a first electrode layer **120200**, an electroluminescent layer **120202**, and a second electrode layer **120203**. The electroluminescent layer **120202** includes a light-emitting material **120201** held by a binder.

An insulating material can be used for the binder. As the insulating material, an organic material or an inorganic material can be used. Alternatively, a mixed material containing an organic material and an inorganic material may be used. As the organic insulating material, a polymer having a comparatively high dielectric constant, such as a cyanoethyl cellulose based resin, or a resin such as polyethylene, polypropylene, a polystyrene based resin, a silicone resin, an epoxy resin, or vinylidene fluoride can be used. Alternatively, a heat-resistant polymer such as aromatic polyamide or polybenzimidazole, or a siloxane resin may be used. Note that a siloxane resin corresponds to a resin having Si—O—Si bonds. Siloxane includes a skeleton structure of a bond of silicon (Si) and oxygen (O). As a substituent, an organic group containing at least hydrogen (such as an alkyl group or aromatic hydrocarbon) is used. Alternatively, a fluoro group, or a fluoro group and an organic group containing at least hydrogen may be used as a substituent. Further alternately, a resin material, for example, a vinyl resin such as polyvinyl alcohol or polyvinylbutyral, a phenol resin, a novolac resin, an acrylic resin, a melamine resin, an urethane resin, or an oxazole resin (polybenzoxazole) may be used. A dielectric constant can be adjusted by appropriately mixing these resins with fine particles having a high dielectric constant, such as barium titanate ($BaTiO_3$) or strontium titanate ($SrTiO_3$).

The inorganic insulating material included in the binder can be formed using silicon oxide (SiO_x), silicon nitride (SiN_x), silicon containing oxygen and nitrogen, aluminum nitride (MN), aluminum containing oxygen and nitrogen, aluminum oxide (Al_2O_3) containing oxygen and nitrogen, titanium oxide (TiO_2), $BaTiO_3$, $SrTiO_3$, lead titanate ($PbTiO_3$), potassium niobate ($KNbO_3$), lead niobate ($PbNbO_3$), tantalum oxide (Ta_2O_5), barium tantalite ($BaTa_2O_6$), lithium tantalite ($LiTaO_3$), yttrium oxide (Y_2O_3), zirconium oxide (ZrO_2), ZnS, or a substance containing another inorganic insulating material. When an inorganic material having a high dielectric constant is included in the organic material (by addition or the like), the dielectric constant of the electroluminescent layer formed of the light-emitting material and the binder can be more effectively controlled, and the dielectric constant can be further increased.

In a manufacturing step, the light-emitting material is dispersed in a solution containing the binder. As a solvent for the solution containing the binder, it is acceptable as long as a solvent dissolves a binder material and can make a solution having a viscosity suitable for a method of forming the electroluminescent layer (various wet processes) and for desired film thickness. For example, an organic solvent or the like can be used as the solvent. When a siloxane resin is used as the binder, propylene glycol monomethyl ether, propylene glycol monomethyl ether acetate (also referred to as PGMEA), 3-methoxy-3-methyl-1-butanol (also referred to as MMB), or the like can be used as the solvent.

The light-emitting elements shown in FIGS. **62**B and **62**C each have a structure where an insulating film is provided between the electrode layer and the electroluminescent layer in the light-emitting element in FIG. **62**A. The light-emitting element shown in FIG. **62**B includes an insulating film **120204** between the first electrode layer **120200** and the electroluminescent layer **120202**. The light-emitting element shown in FIG. **62**C includes an insulating film **120205** between the first electrode layer **120200** and the electroluminescent layer **120202**, and an insulating film **120206** between the second electrode layer **120203** and the electroluminescent layer **120202**. In such a manner, the insulating film may be provided between the electroluminescent layer and one of the electrode layers interposing the electroluminescent layer, or may be provided between the electroluminescent layer and each of the electrode layers interposing the electroluminescent layer. The insulating film may be a single layer or stacked layers including a plurality of layers.

Although the insulating film **120204** is provided in contact with the first electrode layer **120200** in FIG. **62**B, the insulating film **120204** may be provided in contact with the second electrode layer **120203** by reversing the order of the insulating film and the electroluminescent layer.

A material used for an insulating film such as the insulating film **120104** in FIG. **61**B and the insulating film **120204** in FIG. **62**B preferably has high withstand voltage and dense film quality. Further, the material preferably has a high dielectric constant. For example, silicon oxide (SiO_2), yttrium oxide (Y_2O_3), titanium oxide (TiO_2), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), tantalum oxide (Ta_2O_5), barium titanate ($BaTiO_3$), strontium titanate ($SrTiO_3$), lead titanate ($PbTiO_3$), silicon nitride (Si_3N_4), zirconium oxide (ZrO_2), or the like; or a mixed film of these materials or a stacked-layer film including two or more of those materials can be used. The insulating film can be formed by sputtering, evaporation, CVD, or the like. The insulating film may be formed by dispersing particles of the insulating material in a binder. A binder material may be formed using a material and a method similar to those of the binder contained in the electroluminescent layer. The thickness of the insulating film is not particularly limited, but preferably in the range of 10 to 1000 nm.

Note that the light-emitting element can emit light when voltage is applied between the pair of electrode layers interposing the electroluminescent layer. The light-emitting element can operate with DC drive or AC drive.

Note that although this embodiment mode is described with reference to various drawings, the contents (or part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in another drawing. Further, much more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or part of the contents) described in each drawing in this embodiment mode can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in a drawing in another embodiment mode or embodiment. Further, much more drawings can be formed by combining each part in each drawing in this embodiment mode with part of another embodiment mode or embodiment.

Note that this embodiment mode shows examples of embodying, slightly transforming, partially modifying, improving, describing in detail, or applying the contents (or part of the contents) described in other embodiment modes and embodiments, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment mode.

[Embodiment Mode 14]

In this embodiment mode, an example of a display device is described. In particular, the case where optical treatment is performed is described.

A rear projection display device **130100** in FIGS. **63**A and **63**B is provided with a projector unit **130111**, a mirror **130112**, and a screen panel **130101**. The rear projection display device **130100** may also be provided with a speaker **130102** and operation switches **130104**. The projector unit **130111** is provided at a lower portion of a housing **130110** of the rear projection display device **130100**, and projects incident light which projects an image based on a video signal to the mirror **130112**. The rear projection display device **130100** displays an image projected from a rear surface of the screen panel **130101**.

FIG. **64** shows a front projection display device **130200**. The front projection display device **130200** is provided with the projector unit **130111** and a projection optical system **130201**. The projection optical system **130201** projects an image to a screen or the like provided at the front.

Hereinafter, a structure of the projector unit **130111** which is applied to the rear projection display device **130100** in FIGS. **63**A and **63**B and the front projection display device **130200** in FIG. **64** is described.

FIG. **65** shows a structure example of the projector unit **130111**. The projector unit **130111** is provided with a light source unit **130301** and a modulation unit **130304**. The light source unit **130301** is provided with a light source optical system **130303** including lenses and a light source lamp **130302**. The light source lamp **130302** is stored in a housing so that stray light is not scattered. As the light source lamp **130302**, a high-pressure mercury lamp or a xenon lamp, for example, which can emit a large amount of light, is used. The light source optical system **130303** is provided with an optical lens, a film having a function of polarizing light, a film for adjusting phase difference, an IR film, or the like as appropriate. The light source unit **130301** is provided so that emitted light is incident on the modulation unit **130304**. The modulation unit **130304** is provided with a plurality of display panels **130308**, a color filter, a dichroic mirror **130305**, a total reflection mirror **130306**, a prism **130309**, and a projection optical system **130310**. Light emitted from the light source unit **130301** is split into a plurality of optical paths by the dichroic mirror **130305**.

The display panel **130308** and a color filter which transmits light with a predetermined wavelength or wavelength range are provided in each optical path. The transmissive display panel **130308** modulates transmitted light based on a video signal. Light of each color transmitted through the display panel **130308** is incident on the prism **130309**, and an image is displayed on a screen through the projection optical system **130310**. Note that a Fresnel lens may be provided between the mirror and the screen. Then, projected light which is projected by the projector unit **130111** and reflected by the mirror is converted into generally parallel light by the Fresnel lens and projected on the screen.

FIG. **66** shows the projector unit **130111** provided with reflective display panels **130407**, **130408**, and **130409**.

The projector unit **130111** shown in FIG. **66** is provided with the light source unit **130301** and a modulation unit **130400**. The light source unit **130301** may have a structure similar to that of FIG. **65**. Light from the light source unit **130301** is split into a plurality of optical paths by dichroic mirrors **130401** and **130402** and a total reflection mirror **130403** to be incident on polarization beam splitters **130404**, **130405**, and **130406**. The polarization beam splitters **130404**, **130405**, and **130406** are provided corresponding to the reflective display panels **130407**, **130408**, and **130409** which correspond to respective colors. The reflective display panels **130407**, **130408**, and **130409** modulate reflected light based on a video signal. Light of respective colors which is reflected by the reflective display panels **130407**, **130408**, and **130409** is incident on the prism **130109** to be synthesized, and projected through a projection optical system **130411**.

Among light emitted from the light source unit **130301**, only light in a wavelength region of red is transmitted through the dichroic mirror **130401** and light in wavelength regions of green and blue is reflected by the dichroic mirror **130401**. Further, only the light in the wavelength region of green is reflected by the dichroic mirror **130402**. The light in the wavelength region of red, which is transmitted through the dichroic mirror **130401**, is reflected by the total reflection mirror **130403** and incident on the polarization beam splitter **130404**. The light in the wavelength region of blue is incident on the polarization beam splitter **130405**. The light in the wavelength region of green is incident on the polarization beam splitter **130406**. The polarization beam splitters **130404**, **130405**, and **130406** have a function of splitting incident light into p-polarized light and s-polarized light and a function of transmitting only p-polarized light. The reflective display panels **130407**, **130408**, and **130409** polarize incident light based on a video signal.

Only s-polarized light corresponding to respective colors is incident on the reflective display panels **130407**, **130408**, and **130409** corresponding to respective colors. Note that the reflective display panels **130407**, **130408**, and **130409** may be liquid crystal panels. In this case, the liquid crystal panel operates in an electrically controlled birefringence (ECB) mode. Liquid crystal molecules are vertically aligned with respect to a substrate at a certain angle. Accordingly, in the reflective display panels **130407**, **130408**, and **130409**, when a pixel is in an off state, display molecules are aligned so as to reflect incident light without changing a polarization state of the incident light. When the pixel is in an on state, alignment of the display molecules is changed, and the polarization state of the incident light is changed.

The projector unit **130111** in FIG. **66** can be applied to the rear projection display device **130100** in FIGS. **63**A and **63**B and the front projection display device **130200** in FIG. **64**.

FIGS. **67**A to **67**C show single-panel type projector units. The projector unit **130111** shown in FIG. **67**A is provided with the light source unit **130301**, a display panel **130507**, a projection optical system **130511**, and a retardation plate **130504**. The projection optical system **130511** includes one or a plurality of lenses. The display panel **130507** may be provided with a color filter.

FIG. **67**B shows a structure of the projector unit **130111** operating in a field sequential mode. A field sequential mode refers to a mode in which color display is performed by light of respective colors such as red, green, and blue sequentially incident on a display panel with a time lag, without a color filter. High-definition image can be displayed particularly by combination with a display panel with high-speed response to change in input signal. In FIG. **67**B, a rotating color filter plate **130505** including a plurality of color filters with red, green, blue, or the like is provided between the light source unit **130301** and a display panel **130508**.

FIG. **67**C shows a structure of the projector unit **130111** with a color separation method using a micro lens, as a color display method. This method refers to a method in which color display is realized by providing a micro lens array **130506** on a light incident side of a display panel **130509** and emitting light of each color from each direction. The projector unit **130111** employing this method has little loss of light due to a color filter, so that light from the light source unit **130301** can be efficiently utilized. The projector unit **130111** shown in FIG. **67**C is provided with dichroic mirrors **130501**, **130502**, and **130503** so that light of each color is lit to the display panel **130509** from each direction.

Note that although this embodiment mode is described with reference to various drawings, the contents (or part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in another drawing. Further, much more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or part of the contents) described in each drawing in this embodiment mode can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in a drawing in another embodiment mode or embodiment. Further, much more drawings can be formed by combining each part in each drawing in this embodiment mode with part of another embodiment mode or embodiment.

Note that this embodiment mode shows examples of embodying, slightly transforming, partially modifying, improving, describing in detail, or applying the contents (or part of the contents) described in other embodiment modes and embodiments, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment mode.

[Embodiment Mode 15]

In this embodiment mode, an operation of a display device is described.

FIG. **68** shows a structure example of a display device.

A display device **180100** includes a pixel portion **180101**, a signal line driver circuit **180103**, and a scan line driver circuit **180104**. In the pixel portion **180101**, a plurality of signal lines S**1** to Sn extend from the signal line driver circuit **180103** in a column direction. In the pixel portion **180101**, a plurality of scan lines G**1** to Gm extend from the scan line driver circuit **180104** in a row direction. Pixels **180102** are arranged in matrix at each intersection of the plurality of signal lines S**1** to Sn and the plurality of scan lines G**1** to Gm.

The signal line driver circuit **180103** has a function of outputting a signal to each of the signal lines S**1** to Sn. This signal may be referred to as a video signal. The scan line driver circuit **180104** has a function of outputting a signal to each of the scan lines G**1** to Gm. This signal may be referred to as a scan signal.

The pixel **180102** includes at least a switching element connected to the signal line. On/off of the switching element is controlled by a potential of the scan line (a scan signal). When the switching element is turned on, the pixel **180102** is selected. On the other hand, when the switching element is turned off, the pixel **180102** is not selected.

When the pixel **180102** is selected (a selection state), a video signal is input to the pixel **180102** from the signal line. A state (e.g., luminance, transmittance, or voltage of a storage capacitor) of the pixel **180102** is changed in accordance with the video signal input thereto.

When the pixel **180102** is not selected (a non-selection state), the video signal is not input to the pixel **180102**. Note that the pixel **180102** holds a potential corresponding to the video signal which is input when selected; thus, the pixel **180102** maintains the state (e.g., luminance, transmittance, or voltage of a storage capacitor) in accordance with the video signal.

Note that a structure of the display device is not limited to that shown in FIG. **68**. For example, an additional wiring (such as a scan line, a signal line, a power supply line, a capacitor line, or a common line) may be added in accordance with the structure of the pixel **180102**. As another example, a circuit having various functions may be added.

FIG. **69** shows an example of a timing chart for describing an operation of a display device.

The timing chart of FIG. **69** shows one frame period corresponding to a period when an image of one screen is displayed. One frame period is not particularly limited, but is preferably 1/60 second or less so that a viewer does not perceive a flicker.

The timing chart of FIG. **69** shows timing of selecting the scan line G**1** in the first row, the scan line Gi (one of the scan lines G**1** to Gm) in the i-th row, the scan line Gi+1 in the (i+1)th row, and the scan line Gm in the m-th row.

At the same time as the scan line is selected, the pixel **180102** connected to the scan line is also selected. For example, when the scan line Gi in the i-th row is selected, the pixel **180102** connected to the scan line Gi in the i-th row is also selected.

The scan lines G**1** to Gm are sequentially selected (hereinafter also referred to as scanned) from the scan line G**1** in the first row to the scan line Gm in the m-th row. For example, while the scan line Gi in the i-th row is selected, the scan lines (G**1** to Gi−1 and Gi+1 to Gm) other than the scan line Gi in the i-th row are not selected. Then, during the next period, the scan line Gi+1 in the (i+1)th row is selected. Note that a period during which one scan line is selected is referred to as one gate selection period.

Accordingly, when a scan line in a certain row is selected, video signals from the signal lines S**1** to Sn are input to a plurality of pixels **180102** connected to the scan line, respectively. For example, while the scan line Gi in the i-th row is selected, given video signals are input from the signal lines S**1** to Sn to the plurality of pixels **180102** connected to the scan line Gi in the i-th row, respectively. Thus, each of the plurality of pixels **180102** can be controlled individually by the scan signal and the video signal.

Next, the case where one gate selection period is divided into a plurality of subgate selection periods is described. FIG. **70** is a timing chart in the case where one gate selection period is divided into two subgate selection periods (a first subgate selection period and a second subgate selection period).

Note that one gate selection period may be divided into three or more subgate selection periods.

The timing chart of FIG. **70** shows one frame period corresponding to a period when an image of one screen is displayed. One frame period is not particularly limited, but is preferably 1/60 second or less so that a viewer does not perceive a flicker.

Note that one frame is divided into two subframes (a first subframe and a second subframe).

The timing chart of FIG. **70** shows timing of selecting the scan line Gi in the i-th row, the scan line Gi+1 in the (i+1)th row, the scan line Gj (one of the scan lines Gi+1 to Gm) in the j-th row, and the scan line Gj+1 (one of the scan lines Gi+1 to Gm) in the (j+1)th row.

At the same time as the scan line is selected, the pixel **180102** connected to the scan line is also selected. For example, when the scan line Gi in the i-th row is selected, the pixel **180102** connected to the scan line Gi in the i-th row is also selected.

The scan lines G**1** to Gm are sequentially scanned in each subgate selection period. For example, in one gate selection period, the scan line Gi in the i-th row is selected in the first subgate selection period, and the scan line Gj in the j-th row is selected in the second subgate selection period. Thus, in one gate selection period, an operation can be performed as if the scan signals of two rows are selected. At this time, different video signals are input to the signal lines S**1** to Sn in the first subgate selection period and the second subgate selection period. Accordingly, different video signals can be input to a plurality of pixels **180102** connected to the i-th row and a plurality of pixels **180102** connected to the j-th row.

Next, a driving method for displaying images with high quality is described.

FIGS. **71**A and **7113** are views for describing high frequency driving.

FIG. **71**A shows the case where one image and one intermediate image are displayed in one frame period **180400**. Reference numerals **180401**, **180402**, **180403**, and **180404** denote an image of one frame, an intermediate image of the frame, an image of the next frame, and an intermediate image of the next frame, respectively.

The intermediate image **180402** of the frame may be made based on image signals of the frame and the next frame. Alternatively, the intermediate image **180402** of the frame may be made from the image **180401** of the frame, or may be a black image. Accordingly, the quality of a moving image in a hold-type display device can be improved. Further, when one image and one intermediate image are displayed in one frame period **180400**, there is an advantage in that consistency with a frame rate of the video signal can be easily obtained and an image processing circuit is not complicated.

FIG. **7113** shows the case where one image and two intermediate images are displayed in a period with two successive one frame periods **180400** (two frame periods). Reference numeral **180411**, **180412**, **180413**, and **180414** denote an image of the frame, an intermediate image of the frame, an intermediate image of the next frame, an image of a frame after next, respectively.

Each of the intermediate image **180412** of the frame and the intermediate image **180413** of the next frame may be made based on video signals of the frame, the next frame, and the frame after next. Alternatively, each of the intermediate image **180412** of the frame and the intermediate image **180413** of the next frame may be a black image. When one image and two intermediate images are displayed in two frame periods, there is an advantage in that operating frequency of a peripheral driver circuit is not so high and the quality of a moving image can be effectively improved.

Note that although this embodiment mode is described with reference to various drawings, the contents (or part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in another drawing. Further, much more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or part of the contents) described in each drawing in this embodiment mode can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in a drawing in another embodiment mode or embodiment. Further, much more drawings can be formed by combining each part in each drawing in this embodiment mode with part of another embodiment mode or embodiment.

Note that this embodiment mode shows examples of embodying, slightly transforming, partially modifying, improving, describing in detail, or applying the contents (or part of the contents) described in other embodiment modes and embodiments, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment mode.

[Embodiment Mode 16]

In this embodiment mode, a structure of an EL element is described. In particular, a structure of an organic EL element is described.

A structure of a mixed junction EL element is described. As an example, a structure is described, which includes a layer (a mixed layer) in which a plurality of materials among a hole injecting material, a hole transporting material, a light-emitting material, an electron transporting material, an electron injecting material, and the like are mixed (hereinafter referred to as a mixed junction type EL element), which is different from a stacked-layer structure where a hole injecting layer formed of a hole injecting material, a hole transporting layer formed of a hole transporting material, a light-emitting layer formed of a light-emitting material, an electron transporting layer formed of an electron transporting material, an electron injecting layer formed of an electron injecting material, and the like are clearly distinguished.

FIGS. **72**A to **72**E are schematic views each showing a structure of a mixed junction type EL element. Note that a layer interposed between an anode **190101** and a cathode **190102** corresponds to an EL layer.

FIG. **72**A shows a structure in which an EL layer includes a hole transporting region **190103** formed of a hole transporting material and an electron transporting region **190104** formed of an electron transporting material. The hole transporting region **190103** is closer to the anode than the electron transporting region **190104**. A mixed region **190105** including both the hole transporting material and the electron transporting material is provided between the hole transporting region **190103** and the electron transporting region **190104**.

In a direction from the anode **190101** to the cathode **190102**, a concentration of the hole transporting material in the mixed region **190105** is decreased and a concentration of the electron transporting material in the mixed region **190105** is increased.

Note that a concentration gradient can be freely set. For example, a ratio of concentrations of each functional material may be changed (a concentration gradient may be formed) in the mixed region **190105** including both the hole transporting material and the electron transporting material, without including the hole transporting region **190103** formed of only the hole transporting material. Alternatively, a ratio of concentrations of each functional material may be changed (a concentration gradient may be formed) in the mixed region **190105** including both the hole transporting material and the electron transporting material, without including the hole transporting region **190103** formed of only the hole transporting material and the electron transporting region **190104** formed of only the electron transporting material. Further alternatively, a ratio of concentrations may be changed depending on a distance from the anode or the cathode. Note that the ratio of concentrations may be changed continuously.

A region **190106** to which a light-emitting material is added is included in the mixed region **190105**. A light emission color of the EL element can be controlled by the light-emitting material. Further, carriers can be trapped by the light-emitting material. As the light-emitting material, various fluorescent dyes as well as a metal complex having a quinoline skeleton, a benzoxazole skeleton, or a benzothiazole skeleton can be used. The light emission color of the EL element can be controlled by adding the light-emitting material.

As the anode **190101**, an electrode material having a high work function is preferably used in order to inject holes efficiently. For example, a transparent electrode formed of indium tin oxide (ITO), indium zinc oxide (IZO), ZnO, SnO_2, In_2O_3, or the like can be used. When a light-transmitting property is not needed, the anode **190101** may be formed of an opaque metal material.

As the hole transporting material, an aromatic amine compound or the like can be used.

As the electron transporting material, a metal complex having a quinoline derivative, 8-quinolinol, or a derivative thereof as a ligand (especially tris(8-quinolinolato)aluminum (Alq_3)), or the like can be used.

As the cathode **190102**, an electrode material having a low work function is preferably used in order to inject electrons efficiently. A metal such as aluminum, indium, magnesium, silver, calcium, barium, or lithium can be used by itself. Alternatively, an alloy of the aforementioned metal or an alloy of the aforementioned metal and another metal may be used.

FIG. **72**B is the schematic view of the structure of the EL element, which is different from that of FIG. **72**A. Note that the same portions as those in FIG. **72**A are denoted by the same reference numerals, and description thereof is omitted.

In FIG. **72**B, a region to which a light-emitting material is added is not included. However, when a material (electron-transporting and light-emitting material) having both an electron transporting property and a light-emitting property, for example, tris(8-quinolinolato)aluminum (Alq_3) is used as a material added to the electron transporting region **190104**, light emission can be performed.

Alternatively, as a material added to the hole transporting region **190103**, a material (a hole-transporting and light-emitting material) having both a hole transporting property and a light-emitting property may be used.

FIG. **72**C is the schematic view of the structure of the EL element, which is different from those of FIGS. **72**A and **72**B. Note that the same portions as those in FIGS. **72**A and **72**B are denoted by the same reference numerals, and description thereof is omitted.

In FIG. **72**C, a region **190107** included in the mixed region **190105** is provided, to which a hole blocking material having a larger energy difference between the highest occupied molecular orbital and the lowest unoccupied molecular orbital than the hole transporting material is added. The region **190107** to which the hole blocking material is added is provided closer to the cathode **190102** than the region **190106** in the mixed region **190105**, to which the light-emitting material is added; thus, a recombination rate of carriers can be increased, and light emission efficiency can be increased. The structure provided with the region **190107** to which the hole blocking material is added is especially effective in an EL element which utilizes light emission (phosphorescence) by a triplet exciton.

FIG. **72**D is the schematic view of the structure of the EL element, which is different from those of FIGS. **72**A to **72**C. Note that the same portions as those in FIGS. **72**A to **72**C are denoted by the same reference numerals, and description thereof is omitted.

In FIG. **72**D, a region **190108** included in the mixed region **190105** is provided, to which an electron blocking material having a larger energy difference between the highest occupied molecular orbital and the lowest unoccupied molecular orbital than the electron transporting material is added. The region **190108** to which the electron blocking material is added is provided closer to the anode **190101** than the region **190106** in the mixed region **190105**, to which the light-emitting material is added; thus, a recombination rate of carriers can be increased, and light emission efficiency can be increased. The structure provided with the region **190108** to which the electron blocking material is added is especially effective in an EL element which utilizes light emission (phosphorescence) by a triplet exciton.

FIG. **72**E is the schematic view of the structure of the mixed junction type EL element, which is different from those of FIGS. **72**A to **72**D. FIG. **72**E shows an example of a structure where a region **190109** to which a metal material is added is included in part of an EL layer in contact with an electrode of the EL element. In FIG. **72**E, the same portions as those in FIGS. **72**A to **72**D are denoted by the same reference numerals, and description thereof is omitted. In the structure shown in FIG. **72**E, MgAg (an Mg—Ag alloy) may be used as the cathode **190102**, and the region **190109** to which an Al (aluminum) alloy is added may be included in a region of the electron transporting region **190104** to which the electron transporting material is added, which is in contact with the cathode **190102**, for example. With the aforementioned structure, oxidation of the cathode can be prevented, and electron injection efficiency from the cathode can be increased. Accordingly, the lifetime of the mixed junction type EL element can be extended. Further, driving voltage can be lowered.

As a method of forming the mixed junction type EL element, a co-evaporation method or the like can be used.

In the mixed junction type EL elements as shown in FIGS. **72**A to **72**E, a clear interface between the layers does not exist, and charge accumulation can be reduced. Accordingly, the lifetime of the EL element can be extended. Further, driving voltage can be lowered.

Note that the structures shown in FIGS. **72**A to **72**E can be implemented in free combination with each other.

In addition, a structure of the mixed junction type EL element is not limited to those described above. A known structure can be freely used.

An organic material which forms an EL layer of an EL element may be a low molecular material or a high molecular material. Alternatively, both of the materials may be used. When a low molecular material is used for an organic compound material, a film can be formed by an evaporation method. When a high molecular material is used for the EL layer, the high molecular material is dissolved in a solvent and a film can be formed by a spin coating method or an inkjet method.

The EL layer may be formed of a middle molecular material. In this specification, a middle molecule organic light-emitting material refers to an organic light-emitting material without a sublimation property and with a polymerization degree of approximately 20 or less. When a middle molecular material is used for the EL layer, a film can be formed by an inkjet method or the like.

Note that a low molecular material, a high molecular material, and a middle molecular material may be used in combination.

An EL element may utilize either light emission (fluorescence) by a singlet exciton or light emission (phosphorescence) by a triplet exciton.

Next, an evaporation device for manufacturing a display device applicable to the present invention is described with reference to drawings.

A display device applicable to the present invention may be manufactured to include an EL layer. The EL layer is formed including at least partially a material which exhibits electroluminescence. The EL layer may be formed of a plurality of layers having different functions. In this case, the EL layer may be formed of a combination of layers having different functions, which are also referred to as a hole injecting and transporting layer, a light-emitting layer, an electron injecting and transporting layer, and the like.

FIG. **73** shows a structure of an evaporation device for forming an EL layer over an element substrate provided with a transistor. In the evaporation device, a plurality of treatment chambers are connected to transfer chambers **190260** and **190261**. Each treatment chamber includes a loading chamber **190262** for supplying a substrate, an unloading chamber **190263** for collecting the substrate, a heat treatment chamber **190268**, a plasma treatment chamber **190272**, deposition treatment chambers **190269** to **190271** and **190273** to **190275** for depositing an EL material, and a deposition treatment chamber **190276** for forming a conductive film which is formed of aluminum or contains aluminum as its main component as one electrode of an EL element. Gate valves **190277***a* to **190277***m* are provided between the transfer chambers and the treatment chambers, so that the pressure in each treatment chamber can be controlled independently, and cross contamination between the treatment chambers is prevented.

A substrate introduced into the transfer chamber **190260** from the loading chamber **190262** is transferred to a predetermined treatment chamber by an arm type transfer means **190266** capable of rotating. The substrate is transferred from a certain treatment chamber to another treatment chamber by the transfer means **190266**. The transfer chambers **190260** and **190261** are connected by the deposition treatment chamber **190270** at which the substrate is transported by the transfer means **190266** and a transfer means **190267**.

Each treatment chamber connected to the transfer chambers **190260** and **190261** is maintained in a reduced pressure state. Accordingly, in the evaporation device, deposition treatment of an EL layer is continuously performed without exposing the substrate to the room air. A display panel in which formation of the EL layer is finished is deteriorated due to moisture or the like in some cases. Accordingly, in the evaporation device, a sealing treatment chamber **190265** for performing sealing treatment before exposure to the room air in order to maintain the quality is connected to the transfer chamber **190261**. Since the sealing treatment chamber **190265** is under atmospheric pressure or reduced pressure near atmospheric pressure, an intermediate treatment chamber **190264** is also provided between the transfer chamber **190261** and the sealing treatment chamber **190265**. The intermediate treatment chamber **190264** is provided for transporting the substrate and buffering the pressure between the chambers.

An exhaust means is provided in the loading chamber, the unloading chamber, the transfer chamber, and the deposition treatment chamber in order to maintain reduced pressure in the chamber. As the exhaust means, various vacuum pumps such as a dry pump, a turbo-molecular pump, and a diffusion pump can be used.

In the evaporation device of FIG. **73**, the number of treatment chambers connected to the transfer chambers **190260** and **190261** and structures thereof can be combined as appropriate in accordance with a stacked-layer structure of the EL element. An example of a combination is described below.

In the heat treatment chamber **190268**, degasification treatment is performed by heating a substrate over which a lower electrode, an insulating partition wall, or the like is formed. In the plasma treatment chamber **190272**, a surface of the lower electrode is treated with a rare gas or oxygen plasma. This plasma treatment is performed for cleaning the surface, stabilizing a surface state, or stabilizing a physical or chemical state (e.g., a work function) of the surface.

The deposition treatment chamber **190269** is for forming an electrode buffer layer which is in contact with one electrode of the EL element. The electrode buffer layer has a carrier injection property (hole injection or electron injection) and suppresses generation of a short-circuit or a black spot defect of the EL element. Typically, the electrode buffer layer is formed of an organic-inorganic hybrid material, has a resistivity of 5×10^4 to 1×10^6 Ωcm, and is formed having a thickness of 30 to 300 nm. Note that the deposition treatment chamber **190271** is for forming a hole transporting layer.

A light-emitting layer in an EL element has a different structure between the case of emitting single color light and the case of emitting white light. Deposition treatment chambers in the evaporation device are preferably arranged depending on the structure. For example, when three kinds of EL elements each having a different light emission color are formed in a display panel, it is necessary to form light-emitting layers corresponding to respective light emission colors. In this case, the deposition treatment chamber **190270** can be used for forming a first light-emitting layer, the deposition treatment chamber **190273** can be used for forming a second light-emitting layer, and the deposition treatment chamber **190274** can be used for forming a third light-emitting layer. By using different deposition treatment chambers for respective light-emitting layers, cross contamination due to different light-emitting materials can be prevented, and throughput of the deposition treatment can be improved.

Note that three kinds of EL elements each having a different light emission color may be sequentially deposited in each of the deposition treatment chambers **190270**, **190273**, and **190274**. In this case, evaporation is performed by moving a shadow mask depending on a region to be deposited.

When an EL element which emits white light is formed, the EL element is formed by vertically stacking light-emitting layers of different light emission colors. In this case also, the element substrate can be sequentially transferred through the deposition treatment chambers so that each light-emitting layer is formed. Alternatively, different light-emitting layers can be formed continuously in the same deposition treatment chamber.

In the deposition treatment chamber **190276**, an electrode is formed over the EL layer. The electrode can be formed by an electron beam evaporation method or a sputtering method, and preferably by a resistance heating evaporation method.

The element substrate in which formation of the electrode is finished is transferred to the sealing treatment chamber **190265** through the intermediate treatment chamber **190264**. The sealing treatment chamber **190265** is filled with an inert gas such as helium, argon, neon, or nitrogen, and a sealing substrate is attached to a side of the element substrate where the EL layer is formed under the atmosphere so that the EL layer is sealed. In a sealed state, a space between the element substrate and the sealing substrate may be filled with an inert gas or a resin material. The sealing treatment chamber **190265** is provided with a dispenser which draws a sealing material, a mechanical element such as an arm or a fixing stage which fixes the sealing substrate to face the element substrate, a dispenser or a spin coater which fills the chamber with a resin material, or the like.

FIG. **74** shows an internal structure of a deposition treatment chamber. The deposition treatment chamber is maintained in a reduced pressure state. In FIG. **74**, a space interposed between a top plate **190391** and a bottom plate **190392** corresponds to an internal space of the chamber, which is maintained in a reduced pressure state.

One or a plurality of evaporation sources are provided in the treatment chamber. This is because a plurality of evaporation sources are preferably provided when a plurality of layers having different compositions are formed or when different materials are co-evaporated. In FIG. **74**, evaporation sources **190381***a*, **190381***b*, and **190381***c* are attached to an evaporation source holder **190380**. The evaporation source holder **190380** is held by a multi joint arm **190383**. The multi-joint arm **190383** allows the evaporation source holder **190380** to move within its movable range by stretching the joint. Alternatively, the evaporation source holder **190380** may be provided with a distance sensor **190382** to monitor a distance between the evaporation sources **190381***a* to **190381***c* and a substrate **190389** so that an optimal distance for evaporation is controlled. In this case, the multi-joint arm may be capable of moving toward upper and lower directions (Z direction) as well.

The substrate **190389** is fixed by using a substrate stage **190386** and a substrate chuck **190387** together. The substrate stage **190386** may have a structure where a heater is incorporated so that the substrate **190389** can be heated. The substrate **190389** is fixed to the substrate stage **190386** with the support of the substrate chuck **190387** and is transferred. At the time of evaporation, a shadow mask **190390** provided with an opening corresponding to an evaporation pattern can be used when needed. In this case, the shadow mask **190390** is arranged between the substrate **190389** and the evaporation sources **190381***a* to **190381***c*. The shadow mask **190390** adheres to the substrate **190389** or is fixed to the substrate **190389** with a certain interval therebetween by a mask chuck **190388**. When alignment of the shadow mask **190390** is needed, the alignment is performed by arranging a camera in the treatment chamber and providing the mask chuck **190388** with a positioning means which slightly moves in X-Y-θ directions.

Each of the evaporation sources **190381***a* to **190381***c* is provided with an evaporation material supply means which continuously supplies an evaporation material to the evaporation source. The evaporation material supply means includes evaporation material supply sources **190385***a*, **190385***b*, and **190385***c*, which are provided apart from the evaporation sources **190381***a*, **190381***b*, and **190381***c*, and a material supply pipe **190384** which connects the evaporation source and the evaporation material supply source. Typically, the evaporation material supply sources **190385***a* to **190385***c* are provided corresponding to the evaporation sources **190381***a* to **190381***c*. In FIG. **74**, the evaporation material supply source **190385***a* corresponds to the evaporation source **190381***a*, the evaporation material supply source **190385***b* corresponds to the evaporation source **190381***b*, and the evaporation material supply source **190385***c* corresponds to the evaporation source **190381***c*.

As a method for supplying an evaporation material, an airflow transfer method, an aerosol method, or the like can be employed. In an airflow transfer method, impalpable powder of an evaporation material is transferred in airflow to the evaporation sources **190381***a* to **190381***c* by using an inert gas or the like. In an aerosol method, evaporation is performed while material liquid in which an evaporation material is dissolved or dispersed in a solvent is transferred and aerosolized by an atomizer and the solvent in the aerosol is vaporized. In each case, the evaporation sources **190381***a* to **190381***c* are provided with a heating means, and a film is formed over the substrate **190389** by vaporizing the transferred evaporation material. In FIG. **74**, the material supply pipe **190384** can be bent flexibly and is formed of a thin pipe which has enough rigidity not to be transformed even under reduced pressure.

When an airflow transfer method or an aerosol method is employed, film formation may be performed in the deposition treatment chamber under atmospheric pressure or lower, and preferably under a reduced pressure of 133 to 13300 Pa. The pressure can be adjusted while an inert gas such as helium, argon, neon, krypton, xenon, or nitrogen fills the deposition treatment chamber or is supplied (and exhausted at the same time) to the deposition treatment chamber. Note that an oxidizing atmosphere may be employed by introducing a gas such as oxygen or nitrous oxide in the deposition treatment chamber where an oxide film is formed. Alternately, a reducing atmosphere may be employed by introducing a gas such as hydrogen in the deposition treatment chamber where an organic material is deposited.

As another method for supplying an evaporation material, a screw may be provided in the material supply pipe **190384** to continuously push the evaporation material toward the evaporation source.

With this evaporation device, a film can be formed continuously with high uniformity even in the case of a large display panel. Since it is not necessary to supply an evaporation material to the evaporation source every time the evaporation material is run out, throughput can be improved.

Note that although this embodiment mode is described with reference to various drawings, the contents (or part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in another drawing. Further, much more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or part of the contents) described in each drawing in this embodiment mode can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in a drawing in another embodiment mode or embodiment. Further, much more drawings can be formed by combining each part in each drawing in this embodiment mode with part of another embodiment mode or embodiment.

Note that this embodiment mode shows examples of embodying, slightly transforming, partially modifying, improving, describing in detail, or applying the contents (or part of the contents) described in other embodiment modes and embodiments, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment mode.

[Embodiment Mode 17]

In this embodiment mode, examples of electronic devices according to the present invention are described.

FIG. **75** shows a display panel module combining a display panel **900101** and a circuit board **900111**. The display panel **900101** includes a pixel portion **900102**, a scan line driver circuit **900103**, and a signal line driver circuit **900104**. The circuit board **900111** is provided with a control circuit **900112**, a signal dividing circuit **900113**, and the like, for example. The display panel **900101** and the circuit board **900111** are connected by a connection wiring **900114**. An FPC or the like can be used for the connection wiring.

In the display panel **900101**, the pixel portion **900102** and part of peripheral driver circuits (a driver circuit having a low operation frequency among a plurality of driver circuits) may be formed over the same substrate by using transistors, and another part of the peripheral driver circuits (a driver circuit having a high operation frequency among the plurality of driver circuits) may be formed over an IC chip. Then, the IC chip may be mounted on the display panel **900101** by COG (Chip On Glass) or the like. Thus, the area of the circuit board **900111** can be reduced, and a small display device can be obtained. Alternatively, the IC chip may be mounted on the display panel **900101** by using TAB (Tape Automated Bonding) or a printed wiring board. Thus, the area of the display panel **900101** can be reduced, and a display device with a narrower frame can be obtained.

For example, in order to reduce power consumption, a pixel portion may be formed over a glass substrate by using transistors, and all peripheral circuits may be formed over an IC chip. Then, the IC chip may be mounted on a display device by COG or TAB.

A television receiver can be completed with the display panel module shown in FIG. **75**. FIG. **76** is a block diagram showing a main structure of a television receiver. A tuner **900210** receives a video signal and an audio signal. The video signals are processed by an video signal amplifier circuit **900202**; a video signal processing circuit **900203** which converts a signal output from the video signal amplifier circuit **900202** into a color signal corresponding to each color of red, green, and blue; and a control circuit **900212** which converts the video signal into an input specification of a driver circuit. The control circuit **900212** outputs signals to each of the scan line side and the signal line side. When digital driving is performed, a structure may be employed in which a signal dividing circuit **900213** is provided on the signal line side and an input digital signal is divided into m signals (m is a positive integer) to be supplied.

Among the signals received by the tuner **900210**, an audio signal is transmitted to an audio signal amplifier circuit **900205**, and an output thereof is supplied to a speaker **900207** through an audio signal processing circuit **900206**. A control circuit **900208** receives control information on receiving station (receiving frequency) and volume from an input portion **900209** and transmits a signal to the tuner **900210** or the audio signal processing circuit **900206**.

FIG. **77**A shows a television receiver incorporated with a display panel module which is different from FIG. **76**. In FIG. **77**A, a display screen **900302** stored in a housing **900301** is formed using the display panel module. Note that speakers **900303**, an operation switch **900304**, and the like may be provided as appropriate.

FIG. **77**B shows a television receiver in which only a display can be carried wirelessly. A battery and a signal receiver are incorporated in a housing **900312**. The battery drives a display portion **900313** or a speaker portion **900317**. The battery can be repeatedly charged by a charger **900310**. The charger **900310** which is capable of transmitting and receiving a video signal can transmit the video signal to the signal receiver of the display. The housing **900312** is controlled by an operation key **900316**. Alternatively, the device shown in FIG. **77**B can transmit a signal to the charger **900310** from the housing **900312** by operating the operation key **900316**. That is, the device may be an image and audio interactive communication device. Further alternatively, by operating the operation key **900316**, a signal is transmitted to the charger **900310** from the housing **900312**, and another electronic device is made to receive a signal which can be transmitted from the charger **900310**; thus, the device can control communication of another electronic device. That is, the device may be a general-purpose remote control device. The present invention can be applied to the display portion **900313**.

FIG. **78**A shows a module combining a display panel **900401** and a printed wiring board **900402**. The display panel **900401** may be provided with a pixel portion **900403** including a plurality of pixels, a first scan line driver circuit **900404**, a second scan line driver circuit **900405**, and a signal line driver circuit **900406** which supplies a video signal to a selected pixel.

The printed wiring board **900402** is provided with a controller **900407**, a central processing unit (CPU) **900408**, a memory **900409**, a power supply circuit **9004010**, an audio processing circuit **900411**, a transmitting/receiving circuit **900412**, and the like. The printed wiring board **900402** and the display panel **900401** are connected by a flexible printed circuit (FPC) **900413**. The flexible printed circuit (FPC) **900413** may be provided with a capacitor, a buffer circuit, or the like so as to prevent noise on power supply voltage or a signal, and increase in rise time of a signal, Note that the controller **900407**, the audio processing circuit **900411**, the memory **900409**, the central processing unit (CPU) **900408**, the power supply circuit **900410**, or the like can be mounted to the display panel **900401** by using a COG (Chip On Glass) method. By using a COG method, the size of the printed wiring board **900402** can be reduced.

Various control signals are input and output through an interface (I/F) portion **900414** provided for the printed wiring board **900402**. An antenna port **900415** for transmitting and receiving a signal to/from an antenna is provided for the printed wiring board **900402**.

FIG. **78**B is a block diagram of the module shown in FIG. **78**A. The module includes a VRAM **900416**, a DRAM **900417**, a flash memory **900418**, and the like as the memory **900409**. The VRAM **900416** stores data on an image displayed on a panel, the DRAM **900417** stores video data or audio data, and the flash memory **900418** stores various programs.

The power supply circuit **900410** supplies electric power for operating the display panel **900401**, the controller **900407**, the central processing unit (CPU) **900408**, the audio processing circuit **900411**, the memory **900409**, and the transmitting/receiving circuit **900412**. Note that the power supply circuit **900410** may be provided with a current source depending on a panel specification.

The central processing unit (CPU) **900408** includes a control signal generation circuit **900420**, a decoder **900421**, a register **900422**, an arithmetic circuit **900423**, a RAM **900424**, an interface (I/F) portion **900419** for the central processing unit (CPU) **900408**, and the like. Various signals input to the central processing unit (CPU) **900408** via the interface (I/F) portion **900414** are once stored in the register **900422**, and subsequently input to the arithmetic circuit **900423**, the decoder **900421**, and the like. The arithmetic circuit **900423** performs operation based on the signal input thereto so as to designate a location to which various instructions are sent. On the other hand, the signal input to the decoder **900421** is decoded and input to the control signal generation circuit **900420**. The control signal generation circuit **900420** generates a signal including various instructions based on the signal input thereto, and transmits the signal to the location designated by the arithmetic circuit **900423**, specifically the memory **900409**, the transmitting/receiving circuit **900412**, the audio processing circuit **900411**, and the controller **900407**, for example.

The memory **900409**, the transmitting/receiving circuit **900412**, the audio processing circuit **900411**, and the controller **900407** operate in accordance with respective instructions. Hereinafter, the operation is briefly described.

A signal input from an input means **900425** is transmitted via the interface (I/F) portion **900414** to the central processing unit (CPU) **900408** mounted to the printed wiring board **900402**. The control signal generation circuit **900420** converts image data stored in the VRAM **900416** into a predetermined format depending on the signal transmitted from the input means **900425** such as a pointing device or a keyboard, and transmits the converted data to the controller **900407**.

The controller **900407** performs data processing of the signal including the image data transmitted from the central processing unit (CPU) **900408** in accordance with the panel specification, and supplies the signal to the display panel **900401**. The controller **900407** generates an Hsync signal, a Vsync signal, a clock signal CLK, alternating voltage (AC Cont), and a switching signal L/R based on power supply voltage input from the power supply circuit **900410** or various signals input from the central processing unit (CPU) **900408**, and supplies the signals to the display panel **900401**.

The transmitting/receiving circuit **900412** processes a signal which is to be transmitted and received as an electric wave by an antenna **900428**. Specifically, the transmitting/receiving circuit **900412** may include a high-frequency circuit such as an isolator, a band pass filter, a VCO (voltage controlled oscillator), an LPF (low pass filter), a coupler, or a balun. A signal including audio information among signals transmitted and received by the transmitting/receiving circuit **900412** is transmitted to the audio processing circuit **900411** in accordance with an instruction from the central processing unit (CPU) **900408**.

The signal including the audio information which is transmitted in accordance with the instruction from the central processing unit (CPU) **900408** is demodulated into an audio signal by the audio processing circuit **900411** and transmitted to a speaker **900427**. An audio signal transmitted from a microphone **900426** is modulated by the audio processing circuit **900411** and transmitted to the transmitting/receiving circuit **900412** in accordance with an instruction from the central processing unit (CPU) **900408**.

The controller **900407**, the central processing unit (CPU) **900408**, the power supply circuit **900410**, the audio processing circuit **900411**, and the memory **900409** can be mounted as a package of this embodiment mode.

It is needless to say that this embodiment mode is not limited to a television receiver and can be applied to various uses, such as a monitor of a personal computer, and especially as a large display medium such as an information display board at the train station, the airport, or the like, or an advertisement display board on the street.

Next, a structure example of a mobile phone according to the present invention is described with reference to FIG. **79**.

A display panel **900501** is detachably incorporated in a housing **900530**. The shape or the size of the housing **900530** can be changed as appropriate in accordance with the size of the display panel **900501**. The housing **900530** which fixes the display panel **900501** is fitted in a printed wiring board **900531** to be assembled as a module.

The display panel **900501** is connected to the printed wiring board **900531** through an FPC **900513**. The printed wiring board **900531** is provided with a speaker **900532**, a microphone **900533**, a transmitting/receiving circuit **900534**, and a signal processing circuit **900535** including a CPU, a controller, and the like. Such a module, an input means **900536**, and a battery **900537** are combined and stored in a housing **900539**. A pixel portion of the display panel **900501** is provided to be seen from an opening window formed in the housing **900539**.

In the display panel **900501**, the pixel portion and part of peripheral driver circuits (a driver circuit having a low operation frequency among a plurality of driver circuits) may be formed over the same substrate by using transistors, and another part of the peripheral driver circuits (a driver circuit having a high operation frequency among the plurality of driver circuits) may be formed over an IC chip. Then, the IC chip may be mounted on the display panel **900501** by COG (Chip On Glass). Alternatively, the IC chip may be connected to a glass substrate by using TAB (Tape Automated Bonding) or a printed wiring board. With such a structure, power consumption of a display device can be reduced, and operation time of the mobile phone per charge can be extended. Further, reduction in cost of the mobile phone can be realized.

The mobile phone shown in FIG. **79** has various functions such as, but not limited to, a function of displaying various kinds of information (e.g., a still image, a moving image, and a text image); a function of displaying a calendar, a date, the time, and the like on a display portion; a function of operating or editing the information displaying on the display portion; a function of controlling processing by various kinds of software (programs); a function of wireless communication; a function of communicating with another mobile phone, a fixed phone, or an audio communication device by using the wireless communication function; a function of connecting with various computer networks by using the wireless communication function; a function of transmitting or receiving various kinds of data by using the wireless communication function; a function of operating a vibrator in accordance with incoming call, reception of data, or an alarm; and a function of generating a sound in accordance with incoming call, reception of data, or an alarm.

In a mobile phone shown in FIG. **80**, a main body (A) **900601** provided with operation switches **900604**, a microphone **900605**, and the like is connected to a main body (B) **900602** provided with a display panel (A) **900608**, a display panel (B) **900609**, a speaker **900606**, and the like by using a hinge **900610** so that the mobile phone can be opened and closed. The display panel (A) **900608** and the display panel (B) **900609** are placed in a housing **900603** of the main body (B) **900602** together with a circuit board **900607**. Each of pixel portions of the display panel (A) **900608** and the display panel (B) **900609** is arranged to be seen from an opening window formed in the housing **900603**.

Specifications of the display panel (A) **900608** and the display panel (B) **900609**, such as the number of pixels, can be set as appropriate in accordance with functions of a mobile phone **900600**. For example, the display panel (A) **900608** can be used as a main screen and the display panel (B) **900609** can be used as a sub-screen.

A mobile phone according to this embodiment mode can be changed in various modes depending on functions or applications thereof. For example, it may be a camera-equipped mobile phone by incorporating an imaging element in a portion of the hinge **900610**. When the operation switches **900604**, the display panel (A) **900608**, and the display panel (B) **900609** are placed in one housing, the aforementioned effects can be obtained. Further, a similar effect can be obtained when the structure of this embodiment mode is applied to an information display terminal equipped with a plurality of display portions.

The mobile phone in FIG. **80** has various functions such as, but not limited to, a function of displaying various kinds of information (e.g., a still image, a moving image, and a text image); a function of displaying a calendar, a date, the time, and the like on a display portion; a function of operating or editing the information displaying on the display portion; a function of controlling processing by various kinds of software (programs); a function of wireless communication; a function of communicating with another mobile phone, a fixed phone, or an audio communication device by using the wireless communication function; a function of connecting with various computer networks by using the wireless communication function; a function of transmitting or receiving various kinds of data by using the wireless communication function; a function of operating a vibrator in accordance with incoming call, reception of data, or an alarm; and a function of generating a sound in accordance with incoming call, reception of data, or an alarm.

The present invention can be applied to various electronic devices. Specifically, the present invention can be applied to a display portion of an electronic device. Examples of such electronic devices include cameras such as a video camera and a digital camera, a goggle-type display, a navigation system, an audio reproducing device (such as car audio components and audio components), a computer, a game machine, a portable information terminal (such as a mobile computer, a mobile phone, a mobile game machine, and an electronic book), and an image reproducing device provided with a recording medium (specifically, a device which reproduces a recording medium such as a digital versatile disc (DVD) and has a display for displaying the reproduced image).

FIG. **81**A shows a display, which includes a housing **900711**, a support base **900712**, a display portion **900713**, and the like. The display shown in FIG. **81**A can have various functions such as, but not limited to, a function of displaying various kinds of information (e.g., a still image, a moving image, and a text image) on the display portion.

FIG. **81**B shows a camera, which includes a main body **900721**, a display portion **900722**, an image receiving portion **900723**, operation keys **900724**, an external connection port **900725**, a shutter button **900726**, and the like. The camera shown in FIG. **81**B can have various functions such as, but not limited to, a function of photographing a still image and a moving image; a function of automatically adjusting the photographed image (the still image or the moving image); a function of storing the photographed image in a recording medium (provided externally or incorporated in the camera); and a function of displaying the photographed image on the display portion.

FIG. **81**C shows a computer, which includes a main body **900731**, a housing **900732**, a display portion **900733**, a keyboard **900734**, an external connection port **900735**, a pointing device **900736**, and the like. The computer shown in FIG. **81**C can have various functions such as, but not limited to, a function of displaying various kinds of information (e.g., a still image, a moving image, and a text image) on the display portion; a function of controlling processing by various kinds of software (programs); a communication function such as wireless communication or wire communication; a function of connecting with various computer networks by using the communication function; and a function of transmitting or receiving various kinds of data by using the communication function.

FIG. **81**D shows a mobile computer, which includes a main body **900741**, a display portion **900742**, a switch **900743**, operation keys **900744**, an infrared port **900745**, and the like. The mobile computer shown in FIG. **81**D can have various functions such as, but not limited to, a function of displaying various kinds of information (e.g., a still image, a moving image, and a text image) on the display portion; a touch panel function provided on the display portion; a function of displaying a calendar, a date, the time, and the like on the display portion; a function of controlling processing by various kinds of software (programs); a function of wireless communication; a function of connecting with various computer networks by using the wireless communication function; and a function of transmitting or receiving various kinds of data by using the wireless communication function.

FIG. **81**E shows a portable image reproducing device provided with a recording medium (e.g., a DVD reproducing device), which includes a main body **900751**, a housing **900752**, a display portion A **900753**, a display portion B **900754**, a recording medium (e.g., DVD) reading portion **900755**, operation keys **900756**, a speaker portion **900757**, and the like. The display portion A **900753** can mainly display image information, and the display portion B **900754** can mainly display text information.

FIG. **81**F shows a goggle-type display, which includes a main body **900761**, a display portion **900762**, an earphone **900763**, a support portion **900764**, and the like. The goggle-type display shown in FIG. **81**F can have various functions such as, but not limited to, a function of displaying an image (e.g., a still image, a moving image, and a text image) which is externally obtained on the display portion.

FIG. **81**G shows a portable game machine, which includes a housing **900771**, a display portion **900772**, speaker portions **900773**, operation keys **900774**, a recording medium insert portion **900775**, and the like. The portable game machine shown in FIG. **81**G can have various functions such as, but not limited to, a function of reading a program or data stored in the recording medium to display on the display portion; and a function of sharing information by wireless communication with another portable game machine.

FIG. **81**H shows a digital camera having a television reception function, which includes a housing **900781**, a display portion **900782**, operation keys **900783**, a speaker **900784**, a shutter button **900785**, an image receiving portion **900786**, an antenna **900787**, and the like. The digital camera having the television reception function shown in FIG. **81**H can have various functions such as, but not limited to, a function of photographing a still image and a moving image; a function of automatically adjusting the photographed image; a function of obtaining various kinds of information from the antenna; a function of storing the photographed image or the information obtained from the antenna; and a function of displaying the photographed image or the information obtained from the antenna on the display portion.

As shown in FIGS. **81**A to **81**H, the electronic device according to the present invention includes a display portion for displaying some kind of information. In the electronic device according to the present invention, when pieces of data overlap with each other, the overlapping data is stored in a memory; thus, frequency of circuit operations can be decreased. Accordingly, the electronic device has low power consumption and can drive with a battery for a long time.

Next, application examples of the display device according to the present invention are described.

FIG. **82** shows an example in which the display device according to the present invention is incorporated in a constructed object. FIG. **82** shows a housing **900810**, a display portion **900811**, a remote control device **900812** which is an operation portion, a speaker portion **900813**, and the like. The display device according to the present invention is incorporated in the constructed object as a wall-mounted display device, which can be provided without requiring a large space.

FIG. **83** shows another example in which the display device according to the present invention is incorporated in a constructed object. A display panel **900901** is incorporated with a prefabricated bath **900902**, and a person who takes a bath can view the display panel **900901**. The display panel **900901** has a function of displaying information by an operation by the person who takes a bath; and a function of being used as an advertisement or an entertainment means.

Note that the display device according to the present invention can be provided not only to a side wall of the prefabricated bath **900902** as shown in FIG. **83**, but also to various places. For example, the display device can be incorporated with part of a minor, a bathtub itself, or the like. At this time, the shape of the display panel **900901** may be changed in accordance with the shape of the mirror or the bathtub.

FIG. **84** shows another example in which the display device according to the present invention is incorporated in a constructed object. A display panel **901002** is bent and attached to a curved surface of a column-shaped object **901001**. Note that here, a utility pole is described as the column-shaped object **901001**.

The display panel **901002** shown in FIG. **84** is provided at a position higher than a human viewpoint. When the display panels **901002** are provided in constructed objects which stand together in large numbers outdoors, such as utility poles, advertisement can be performed to an unspecified number of viewers. Since it is easy for the display panels **901002** to display the same images and instantly switch images by external control, highly efficient information display and advertisement effect can be obtained. By provision of self-luminous display elements, the display panel **901002** can be useful as a highly visible display medium even at night. When the display panel **901002** is provided in the utility pole, a power supply means for the display panel **901002** can be easily obtained. In an emergency such as disaster, the display panel **901002** can also be used as a means to transmit correct information to victims rapidly.

Note that an example of the display panel **901002** includes a display panel in which a switching element such as an organic transistor is provided over a film-shaped substrate and a display element is driven so that an image is displayed.

Note that in this embodiment mode, a wall, a column-shaped object, and a prefabricated bath are shown as examples of constructed objects; however, this embodiment mode is not limited thereto, and various constructed objects can be provided with the display device according to the present invention.

Next, examples where the display device according to the present invention is incorporated with a moving object are described.

FIG. **85** shows an example in which the display device according to the present invention is incorporated with a car. A display panel **901101** is incorporated with a car body **901102** and can display an operation of the car body or information input from inside or outside the car body on demand. Note that a navigation function may be provided.

The display device according to the present invention can be provided not only to the car body **901102** as shown in FIG. **85**, but also to various places. For example, the display device can be incorporated with a glass window, a door, a steering wheel, a gear shift, a seat, a rear-view mirror, and the like. At this time, the shape of the display panel **901101** may be changed in accordance with the shape of an object provided with the display device.

FIGS. **86**A and **86**B show examples where the display device according to the present invention is incorporated with a train car.

FIG. **86**A shows an example in which a display panel **901202** is provided in glass of a door **901201** in a train car, which has an advantage compared with a conventional advertisement using paper in that labor cost for changing an advertisement is not necessary. Since the display panel **901202** can instantly switch images displaying on a display portion by an external signal, images on the display panel can be switched in every time period when types of passengers on the train are changed, for example. Thus, a more effective advertisement effect can be obtained.

FIG. **86**B shows an example in which the display panels **901202** are provided to a glass window **901203** and a ceiling **901204** as well as the glass of the door **901201** in the train car. In such a manner, the display device according to the present invention can be easily provided to a place where a display device has been difficult to be provided conventionally; thus, an effective advertisement effect can be obtained. Further, the display device according to the present invention can instantly switch images displayed on a display portion by an external signal; thus, cost and time for changing an advertisement can be reduced, and more flexible advertisement management and information transmission can be realized.

Note that the display device according to the present invention can be provided not only to the door **901201**, the glass window **901203**, and the ceiling **901204** as shown in FIGS. **86**A and **86**B, but also to various places. For example, the display device can be incorporated with a strap, a seat, a handrail, a floor, and the like. At this time, the shape of the display panel **901202** may be changed in accordance with the shape of an object provided with the display device.

FIGS. **87**A and **87**B show an example in which the display device according to the present invention is incorporated with a passenger airplane.

FIG. **87**A shows the shape of a display panel **901302** provided on a ceiling **901301** above a seat of the passenger airplane when the display panel **901302** is used. The display panel **901302** is incorporated with the ceiling **901301** with a hinge portion **901303**, and a passenger can view the display panel **901302** by stretching of the hinge portion **901303**. The display panel **901302** has a function of displaying information by an operation by the passenger and a function of being used for an advertisement or an entertainment means. As shown in FIG. **87**B, when the hinge portion is bent so that the display panel is stored in the ceiling **901301**, safety in taking-off and landing can be assured. Note that in an emergency, the display panel can also be used for an information transmission means and a guide light by lighting a display element in the display panel.

Note that the display device according to the present invention can be provided not only to the ceiling **901301** as shown in FIGS. **87**A and **87**B, but also to various places. For example, the display device can be incorporated with a seat, a table attached to a seat, an armrest, a window, and the like. A large display panel which a plurality of people can view may be provided on a wall of an airframe. At this time, the shape of the display panel **901302** may be changed in accordance with the shape of an object provided with the display device.

Note that in this embodiment mode, bodies of a train car, a car, and an airplane are shown as moving objects; however, the present invention is not limited thereto, and the display device according to the present invention can be provided to various objects such as a motorcycle, an four-wheel drive car (including a car, a bus, and the like), a train (including a monorail, a railroad car, and the like), and a vessel. Since the display device according to the present invention can instantly switch images displayed on a display panel in a moving object by an external signal, the moving object provided with the display device according to the present invention can be used as an advertisement display board for an unspecified number of customers, an information display board in disaster, and the like.

Note that although this embodiment mode is described with reference to various drawings, the contents (or part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in another drawing. Further, much more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or part of the contents) described in each drawing in this embodiment mode can be freely applied to, combined with, or replaced with the contents (or part of the contents) described in a drawing in another embodiment mode or embodiment. Further, much more drawings can be formed by combining each part in each drawing in this embodiment mode with part of another embodiment mode or embodiment.

Note that this embodiment mode shows examples of embodying, slightly transforming, partially modifying, improving, describing in detail, or applying the contents (or part of the contents) described in other embodiment modes and embodiments, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment mode.

[Embodiment 1]

In this embodiment, a more specific example of the signal line driver circuit included in the display device shown in FIG. **1** is described.

FIG. **14** shows an example of a circuit diagram of the signal line driver circuit. The signal line driver circuit shown in FIG. **14** includes a shift register **501**, a sampling circuit **502**, a first latch **503**, a second latch **504**, a third latch **505**, a level shifter **506**, and a buffer **507**. Note that although a signal line driver circuit including three latches of the first latch **503**, the second latch **504**, and the third latch **505** as memory circuits is described as an example in this embodiment, the number of memory circuits is not limited to this.

The shift register **501** includes a plurality of delay flip flops (DFFs) **508**. The shift register **501** generates a timing signal, a pulse of which is sequentially shifted, in accordance with the start pulse signal S-SP and the clock signal S-CLK which are input, and the timing signal is input to the sampling circuit **502** in the next stage.

The sampling circuit **502** includes a plurality of memory elements (LATs) **509**. The sampling circuit **502** sequentially samples video signals in accordance with the pulse of the input timing signal, and data of the sampled video signals is written to the memory elements **509**.

The first latch **503** includes a plurality of memory elements (LATs) **510**. The second latch **504** includes a plurality of memory elements (LATs) **511**. The third latch **505** includes a plurality of memory elements (LATs) **512**. The number of each of the memory elements **510**, the memory elements **511**, and the memory elements **512** is preferably the same as or more than the number of pixels of one line in a pixel portion.

The writing latch signal WS_1 and the reading latch signal RS_1 are input to the first latch **503**. The writing latch signal WS_2 and the reading latch signal RS_2 are input to the second latch **504**. The writing latch signal WS_3 and the reading latch signal RS_3 are input to the third latch **505**.

The data which is written to the memory element **509** in the sampling circuit **502** is written to and held in the memory elements **510** included in the first latch **503**, the memory elements **511** included in the second latch **504**, or the memory elements **512** included in the third latch **505**. Writing of the data to the memory elements **510** is controlled by the writing latch signal WS_1; writing of the data to the memory elements **511** is controlled by the writing latch signal WS_2; and writing of the data to the memory elements **512** is controlled by the writing latch signal WS_3.

The data held in the memory elements **510**, the memory elements **511**, or the memory elements **512** is input to the level shifter **506** in the next stage as a video signal. Input of the video signal to the level shifter **506** is controlled by the reading latch signals RS_1 to RS_3.

The level shifter **506** controls voltage amplitude of the input video signal and inputs the input video signal to the buffer **507** in the next stage. The buffer **507** shapes a waveform of the input video signal and input the video signal to the pixel portion.

Although this embodiment is described with reference to various drawings, the contents (or may be part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in another drawing. Further, even more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or may be part of the contents) described in each drawing of this embodiment can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in a drawing in another embodiment mode or embodiment. Further, even more drawings can be formed by combining each part with part of another embodiment mode or embodiment in the drawings of this embodiment.

This embodiment shows an example of an embodied case of the contents (or may be part of the contents) described in other embodiment modes and embodiments, an example of slight transformation thereof, an example of partial modification thereof, an example of improvement thereof, an example of detailed description thereof, an application example thereof, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment.

[Embodiment 2]

In this embodiment, a more specific example of the signal line driver circuit included in the display device shown in FIG. **12** is described.

FIG. **15** shows an example of a circuit diagram of the signal line driver circuit. The signal line driver circuit shown in FIG. **15** includes a shift register **601**, a sampling circuit **602**, a first latch **603**, a second latch **604**, a third latch **605**, and a D/A converter circuit **606**. Note that a signal line driver circuit including three latches of the first latch **603**, the second latch **604**, and the third latch **605** as memory circuits is described as an example in this embodiment, the number of memory circuits is not limited to this.

The shift register **601** includes a plurality of delay flip flops (DFFs) **608**. The shift register **601** generates a timing signal, a pulse of which is sequentially shifted, in accordance with a start pulse signal S-SP and a clock signal S-CLK which are input, and the timing signal is input to the sampling circuit **602** in the next stage.

The sampling circuit **602** includes a plurality of memory elements (LATs) **609**. The number of the memory elements **609** is preferably the same as or more than the number obtained by multiplying the number of pixels of one line in a pixel portion by the number of bits of a video signal. Note that although an example in which the number of bits of the video signal is three is described in FIG. **15**, the number of bits of the video signal is not limited to this. The sampling circuit **602** sequentially samples video signals in accordance with the pulse of the input timing signal, and data of the sampled video signals is written to the memory elements **609**.

The first latch **603** includes a plurality of memory elements (LATs) **610**. The second latch **604** includes a plurality of memory elements (LATs) **611**. The third latch **605** includes a plurality of memory elements (LATs) **612**. The number of each of the memory elements **610**, the memory elements **611**, and the memory elements **612** is preferably the same as or more than the number obtained by multiplying the number of pixels of one line in the pixel portion by the number of bits of the video signal.

The writing latch signal WS_1 and the reading latch signal RS_1 are input to the first latch **603**. The writing latch signal WS_2 and the reading latch signal RS_2 are input to the second latch **604**. The writing latch signal WS_3 and the reading latch signal RS_3 are input to the third latch **605**.

The data which is written to the memory element **609** in the sampling circuit **602** is written to and is held in the memory elements **610** included in the first latch **603**, the memory elements **611** included in the second latch **604**, or the memory elements **612** included in the third latch **605**. Writing of the data to the memory elements **610** is controlled by the writing latch signal WS_1; writing of the data to the memory elements **611** is controlled by the writing latch signal WS_2; and writing of the data to the memory elements **612** is controlled by the writing latch signal WS_3.

Then, the data held in the memory elements **610**, the memory elements **611**, or the memory elements **612** is input to the D/A converter circuit **606** in the next stage as a video signal. Input of the video signal to the D/A converter circuit **606** is controlled by the reading latch signals RS_1 to RS_3. The D/A converter circuit **606** converts the input video signal into an analog video signal and inputs it to the pixel portion in the next stage.

Although this embodiment is described with reference to various drawings, the contents (or may be part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in another drawing. Further, even more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or may be part of the contents) described in each drawing of this embodiment can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in a drawing in another embodiment mode or embodiment. Further, even more drawings can be formed by combining each part with part of another embodiment mode or embodiment in the drawings of this embodiment.

This embodiment shows an example of an embodied case of the contents (or may be part of the contents) described in other embodiment modes and embodiments, an example of slight transformation thereof, an example of partial modification thereof, an example of improvement thereof, an example of detailed description thereof, an application example thereof, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment.

[Embodiment 3]

In this embodiment, a structure of a memory element in a memory circuit included in a display device of the present invention is described.

FIG. **20** shows an example of a circuit diagram of the memory element. FIG. **20** shows structures of memory elements **801** to **803** included in three memory circuits, respectively. The memory element **802** is connected to the next stage of the memory element **801**. The memory element **803** is connected to the next stage of the memory element **802**. Note that although the number of memory elements included in each memory circuit is one in FIG. **20**, the number of memory elements included in each memory circuit is actually the same as or more than the number of pixels of one line. In the case where a digital video signal is converted into an analog video signal in a signal line driver circuit, the number of memory elements included in each circuit is the same as or more than the number obtained by multiplying the number of pixels of one line by the number of bits of the video signal.

The writing latch signal WS_1 and the reading latch signal RS_1 are input to the memory element **801**. The writing latch signal WS_2 and the reading latch signal RS_2 are input to the memory element **802**. The writing latch signal WS_3 and a reading latch signal RS_3 are input to the memory elements **803**.

Since the memory elements **801** to **803** have the same circuit structure in FIG. **20**, the structure of each memory element is described in more detail by giving the memory element **801** as an example.

The memory element **801** includes a clocked inverter **804**, a clocked inverter **806**, an inverter **805**, and a switching circuit **807**. Operations of the clocked inverter **804** and the clocked inverter **806** are controlled by the writing latch signal WS_1 input to the clocked inverter **804** and the clocked inverter **806**. A sampled video signal is input from a sampling circuit to the clocked inverter **804**. Output of the clocked inverter **804** is supplied to the inverter **805**. The inverter **805** and the clocked inverter **806** form a flip-flop circuit by supplying output of the inverter **805** to input of the clocked inverter **806** and supplying output of the clocked inverter **806** to input of the inverter **805**. In addition, the output of the inverter **805** is supplied to the next stage of the memory circuit, e.g., a signal line of a pixel portion or a D/A converter circuit through the switching circuit **807**.

An operation of the switching circuit **807** is controlled by the reading latch signal RS_1 input to the switching circuit **807**. FIG. **20** shows an example in which the switching circuit **807** includes a transmission gate **808** and an inverter **809**. The reading latch signal RS_1 and a signal obtained by inverting the reading latch signal RS_1 by the inverter **809** are input to the transmission gate **808**, and switching of the transmission gate **808** is controlled by these signals.

The contents (or may be part of the contents) described in each drawing of this embodiment can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in a drawing in another embodiment mode or embodiment. Further, even more drawings can be formed by combining each part with part of another embodiment mode or embodiment in the drawings of this embodiment.

This embodiment shows an example of an embodied case of the contents (or may be part of the contents) described in other embodiment modes and embodiments, an example of slight transformation thereof, an example of partial modification thereof, an example of improvement thereof, an example of detailed description thereof, an application example thereof, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment.

[Embodiment 4]

In this embodiment, a structure of a pixel portion included in an active matrix light-emitting device which is a kind of a display device of the present invention is described.

An active matrix light-emitting device includes a light-emitting element which corresponds to a display element in each pixel. Since a light-emitting element emits light by itself, the light-emitting element has high visibility, dose not need a backlight which is necessary for a liquid crystal display device, is suitable for reduction in thickness, and does not have limitations on the viewing angle. Although a light-emitting device using an organic light-emitting element (OLED) which is a kind of a light-emitting element is described in this embodiment, the present invention may be a light-emitting device using another light-emitting element.

An OLED includes a layer including a material in which luminescence (electroluminescence) generated by application of an electric field can be obtained, an anode layer, and a cathode layer. As electroluminescence, there are luminescence (fluorescence) at the time of returning to a ground state from a singlet-excited state and luminescence (phosphorescence) at the time of returning to a ground state from a triplet-excited state. A light-emitting device of the present invention may use either one of fluorescence and phosphorescence or both fluorescence and phosphorescence.

FIG. **16**A is an enlarged view of a pixel portion **301** of a light-emitting device of this embodiment. The pixel portion **301** includes a plurality of pixels **304** arranged in matrix. Reference signs S**1** to Sx denote signals lines; reference signs V**1** to Vx denote power supply lines; and reference signs G**1** to Gy denote scan lines. In this embodiment, the pixel **304** includes one of the signal lines S**1** to Sx, one of the power supply lines V**1** to Vx, and one of the scan lines G**1** to Gy.

FIG. **16**B is an enlarged view of the pixel **304**. In FIG. **16**B, a reference numeral **305** denotes a switching transistor. A gate electrode of the switching transistor **305** is connected to a scan line Gj (j=one of 1 to y). One of a source region and a drain region of the switching transistor **305** is connected to a signal line Si (i=one of 1 to x). The other of the source region and the drain region of the switching transistor **305** is connected to a gate electrode of a driving transistor **306**. In addition, a storage capacitor **308** included in each pixel is provided between a power supply line Vi (i=one of 1 to x) and the gate electrode of the driving transistor **306**.

The storage capacitor **308** is provided to hold gate voltage (a potential difference between the gate electrode and a source region) of the driving transistor **306** when the switching transistor **305** is off. Note that although the structure in which the storage capacitor **308** is provided is described in this embodiment, the present invention is not limited to this structure and the storage capacitor **308** is not necessarily provided.

One of the source region and a drain region of the driving transistor **306** is connected to the power supply line Vi (i=one of 1 to x). The other of the source region and the drain region of the driving transistor **306** is connected to a light-emitting element **307**. The light-emitting element **307** includes an anode, a cathode, and an electroluminescent layer provided between the anode and the cathode. When the anode is connected to the source region or the drain region of the driving transistor **306**, the anode corresponds to a pixel electrode and the cathode corresponds to a counter electrode. Alternatively, when the cathode is connected to the source region or the drain region of the driving transistor **306**, the cathode corresponds to the pixel electrode and the anode corresponds to the counter electrode.

Predetermined voltage is applied to each of the counter electrode of the light-emitting element **307** and the power supply line Vi.

The scan line Gj is selected in accordance with pulses of selection signals input to the scan lines G**1** to Gy from a scan line driver circuit. That is, when the pixel **304** of a line corresponding to the scan line Gj is selected, the switching transistor **305**, the gate electrode of which is connected to the scan line Gj, in the pixel **304** of the line is turned on. Then, when a video signal is input to the signal line Si, the gate voltage of the driving transistor **306** is determined in accordance with voltage of the video signal. When the driving transistor **306** is turned on, the power supply line Vi and the light-emitting element **307** are electrically connected, so that the light-emitting element **307** emits light by supply of current. Alternatively, when the driving transistor **306** is turned off, the power supply line Vi and the light-emitting element **307** are not electrically connected, so that supply of current to the light-emitting element **307** is not performed and the light-emitting element **307** does not emit light.

Note that the switching transistor **305** and the driving transistor **306** can be either n-channel transistors or p-channel transistors. Note that when the source region or the drain region of the driving transistor **306** is connected to the anode of the light-emitting element **307**, the driving transistor **306** is preferably a p-channel transistor. Alternatively, when the source region or the drain region of the driving transistor **306** is connected to the cathode of the light-emitting element **307**, the driving transistor **306** is preferably an n-channel transistor.

Each of the switching transistor **305** and the driving transistor **306** may have a multi-gate structure such as a double-gate structure or a triple-gate structure instead of a single-gate structure.

Note that the present invention can be applied to not only a display device including pixels having the circuit structure shown in FIGS. **16**A and **16**B but also a display device including pixels having various circuit structures. The pixel included in the display device of the present invention may have a threshold voltage compensation circuit structure in which the threshold voltage of the driving transistor can be compensated, a current input circuit structure in which the threshold voltage and mobility of the driving transistor can be compensated by input of current, or the like, for example.

The contents (or may be part of the contents) described in each drawing of this embodiment can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in a drawing in another embodiment mode or embodiment, Further, even more drawings can be formed by combining each part with part of another embodiment mode or embodiment in the drawings of this embodiment.

This embodiment shows an example of an embodied case of the contents (or may be part of the contents) described in other embodiment modes and embodiments, an example of slight transformation thereof, an example of partial modification thereof, an example of improvement thereof, an example of detailed description thereof, an application example thereof, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment.

[Embodiment 5]

In this embodiment, a structure of a pixel portion included in an active matrix liquid crystal display device which is a kind of a display device of the present invention is described.

FIG. **17** is an enlarged view of a pixel portion **401** of a liquid crystal display device of the present invention. In FIG. **17**, the pixel portion **401** includes a plurality of pixels **402** arranged in matrix. Reference signs S**1** to Sx denote signals lines, and reference signs G**1** to Gy denote scan lines. In this embodiment, the pixel **402** includes one of the signal lines S**1** to Sx and one of the scan lines G**1** to Gy.

The pixel **402** includes a transistor **403** functioning as a switching element, a liquid crystal cell **404** corresponding to a display element, and a storage capacitor **405**. The liquid crystal cell **404** includes a pixel electrode, a counter electrode, and liquid crystals held between the pixel electrode and the counter electrode. A gate electrode of the transistor **403** is connected to a scan line Gj (j=one of 1 to x). One of a source region and a drain region of the transistor **403** is connected to a signal line Si (i=one of 1 to x). The other of the source region and the drain region of the transistor **403** is connected to the pixel electrode of the liquid crystal cell **404**. In addition, one of two electrodes of the storage capacitor **405** is connected to the pixel electrode of the liquid crystal cell **404**. The other of the two electrodes of the storage capacitor **405** is connected to a common electrode. The common electrode may be connected to either the counter electrode of the liquid crystal cell **404** or another scan line.

The scan line Gj is selected in accordance with pulses of selection signals input to the scan lines G**1** to Gy from a scan line driver circuit. That is, when the pixel **402** of a line corresponding to the scan line Gj is selected, the transistor **403**, the gate electrode of which is connected to the scan line Gj, in the pixel **402** of the line is turned on. Then, when a video signal is input to the signal line Si from a signal line driver circuit, voltage is applied between the pixel electrode and the counter electrode of the liquid crystal cell in accordance with the video signal. Transmissivity of the liquid crystal cell **404** is determined in accordance with a level of the voltage applied between the pixel electrode and the counter electrode. In addition, the voltage between the pixel electrode and the counter electrode of the liquid crystal cell **404** is held in the storage capacitor **405**.

The contents (or may be part of the contents) described in each drawing of this embodiment can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in a drawing in another embodiment mode or embodiment. Further, even more drawings can be formed by combining each part with part of another embodiment mode or embodiment in the drawings of this embodiment.

This embodiment shows an example of an embodied case of the contents (or may be part of the contents) described in other embodiment modes and embodiments, an example of slight transformation thereof, an example of partial modification thereof, an example of improvement thereof, an example of detailed description thereof, an application example thereof, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment.

[Embodiment 6]

In this embodiment, timing during which video signals are input to a pixel portion in one frame period is described with reference to FIGS. **13**A and **13**B.

FIG. **13**A is a timing chart showing timing during which videos signal are input to a pixel portion when one frame period is divided into subframe periods SF**1** to SF**6**. The horizontal axis represents time and the vertical axis represents a scanning direction of a line selected by a scan line driver circuit. FIG. **13**A shows an example in which a 6-bit video signal is used and one frame period is divided into six (the same number as the number of bits) subframe periods. Note that the number of bits of the video signal is not limited to six in the present invention.

Each of the subframe periods SF**1** to SF**6** includes a writing period Ta for inputting a video signal to each pixel. In the writing period Ta, pixels of respective lines are sequentially selected by the scan line driver circuit. Then, a video signal is input to the pixels of the selected line from a signal line driver circuit. Then, display is performed in accordance with the video signal sequentially from the pixels of the line in which input of the video signal is completed. When input of the video signals to the pixels of all the lines is completed, the writing period is completed. Note that since a video signal for one bit is input to the pixel portion in one writing period, completion of all the writing periods Ta corresponds to completion of input of the 6-bit video signal.

Then, when one writing period is completed, display is continuously performed in accordance with video signal input to the pixel portion until writing period of the next subframe period appears. Next, a writing period corresponding to another subframe period appears, and the above-described operation is repeated. Then, when all the subframe periods sequentially appear, one frame period is formed.

When all the subframe periods in one frame period appear, an image having gray scale levels can be displayed. The number of gray scales can be determined by controlling luminance of a display element in each subframe period. For example, when 64 gray scale levels are displayed by a 6-bit video signal, the ratio of the length of the subframe periods SF**1** to SF**6** is $2^5:2^4:2^3:2^2:2^1:2^0$ sequentially from the longest when the number of gray scale levels is changed linearly.

Note that although luminance of the display element included in the pixel is controlled in accordance with the video signal in the above-described operation, the present invention is not limited to this structure. For example, a non-display period during which luminance of the display element is forcibly made the lowest regardless of a video signal may be provided. Note that the non-display period is not necessarily provided. However, when the length of the subframe period is shorter than the length of the writing period, it is necessary to provide a non-display period as described above. When a non-display period is provided, there is no need for concurrently inputting video signals to pixels of two or more rows in the pixel portion.

Note that operations may be performed by further dividing one subframe period into a plurality of subframe periods. In this case, each of the divided subframe periods includes the writing period Ta.

Next, the case is described in which only one writing period Ta appears in one frame period. FIG. **13**B is a timing chart showing timing during which video signals are input to a pixel portion. The horizontal axis represents time and the vertical axis represents a scanning direction of a line selected by a scan line driver circuit.

In FIG. **13**B, pixels of respective lines are sequentially selected by the scan line driver circuit in the writing period Ta. Then, an analog video signal is input to the pixels of the selected line from a signal line driver circuit. Then, in the writing period Ta, display is performed in accordance with the video signal sequentially from the pixels of the line in which input of the video signal is completed. When input of the video signals to the pixels of all the lines is completed, the writing period is completed. Next, display is performed in accordance with the video signal input to the pixel portion in the writing period Ta until the next frame period appears.

Note that the length of the writing period Ta in FIG. **13**B can be set as appropriate by a designer as long as it is within one frame period. When the length of the writing period Ta is approximately the same as one frame period, driving frequency of the signal line driver circuit at the time of writing the video signal can be reduced and power consumption can also be reduced.

The contents (or may be part of the contents) described in each drawing of this embodiment can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in a drawing in another embodiment mode or embodiment. Further, even more drawings can be formed by combining each part with part of another embodiment mode or embodiment in the drawings of this embodiment.

This embodiment shows an example of an embodied case of the contents (or may be part of the contents) described in other embodiment modes and embodiments, an example of slight transformation thereof, an example of partial modification thereof, an example of improvement thereof, an example of detailed description thereof, an application example thereof, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment.

[Embodiment 7]

In this embodiment mode, a light-emitting device which is a kind of a display device of the present invention is given as an example, and an appearance thereof is described with reference to FIGS. **18**A and **18**B. FIG. **18**A is a top plan view of a panel in which a transistor and a light-emitting element formed over a first substrate are sealed between the first substrate and a second substrate by a sealant. FIG. **18**B corresponds to a cross-sectional view taken along a line A-A' in FIG. **18**A.

A sealant **4020** is provide so as to surround a pixel portion **4002**, a signal line driver circuit **4003**, and a scan line driver circuit **4004** which are provided over a first substrate **4001**. A second substrate **4006** is provided over the pixel portion **4002**, the signal line driver circuit **4003**, and the scan line driver circuit **4004**. Thus, the pixel portion **4002**, the signal line driver circuit **4003**, and the scan line driver circuit **4004** are sealed between the first substrate **4001** and the second substrate **4006** together with a filler **4007** by the sealant **4020**.

Each of the pixel portion **4002**, the signal line driver circuit **4003**, and the scan line driver circuit **4004** which are provided over the first substrate **4001** includes a plurality of transistors. FIG. **18**B illustrates a transistor **4008** included in the signal line driver circuit **4003**, and a driving transistor **4009** and a switching transistor **4010** which are included in the pixel portion **4002**.

A light-emitting element **4011** uses part of a wiring **4017** connected to a source region or a drain region of the driving transistor **4009** as a pixel electrode. In addition, the light-emitting element **4011** includes a counter electrode **4012** and an electroluminescent layer **4013** as well as the pixel electrode. Note that the structure of the light-emitting element **4011** is not limited to the structure shown in this embodiment. The structure of the light-emitting element **4011** can be changed as appropriate in accordance with a direction of light extracted from the light-emitting element **4011**, polarity of the driving transistor **4009**, or the like.

Although various signals and voltages supplied to the pixel portion **4002**, the signal line driver circuit **4003**, or the scan line driver circuit **4004** are not shown in the cross-sectional view in FIG. **18**B, various signals and voltages are supplied from a connection terminal **4016** through extraction wirings **4014** and **4015**.

In this embodiment, the connection terminal **4016** is formed using the same conductive film as the counter electrode **4012** included in the light-emitting element **4011**. The extraction wiring **4014** is formed using the same conductive film as the wiring **4017**. The extraction wiring **4015** is formed using the same conductive film as gate electrodes included in the driving transistor **4009**, the switching transistor **4010**, and the transistor **4008**, respectively.

The connection terminal **4016** is electrically connected to a terminal included in an FPC **4018** through an anisotropic conductive film **4019**.

Glass, metal (typically, stainless steel), ceramic, or plastic can be used for the first substrate **4001** and the second substrate **4006**. Note that the second substrate **4006** located in the direction of light extracted from the light-emitting element **4011** necessarily has light-transmitting properties. Thus, a light-transmitting material such as a glass plate, a plastic plate, a polyester film, or an acryl film is preferably used for the second substrate **4006**.

In addition, an ultraviolet curable resin or a thermoset resin can be used for the filler **4007** as well as inert gas such as nitrogen or argon. In this embodiment, an example in which nitrogen is used for the filler **4007** is described.

Although this embodiment is described with reference to various drawings, the contents (or may be part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in another drawing. Further, even more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or may be part of the contents) described in each drawing of this embodiment can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in a drawing in another embodiment mode or embodiment. Further, even more drawings can be formed by combining each part with part of another embodiment mode or embodiment in the drawings of this embodiment.

This embodiment shows an example of an embodied case of the contents (or may be part of the contents) described in other embodiment modes and embodiments, an example of slight transformation thereof, an example of partial modification thereof, an example of improvement thereof, an example of detailed description thereof, an application example thereof, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment.

[Embodiment 8]

Since power consumption of a display device of the present invention can be suppressed, the display device of the present invention is suitable for a display portion included in a hand-held portable electronic device such as a mobile phone, a portable game machine, an electronic book, a video camera, or a digital still camera.

As an electronic device which can use the display device of the present invention, a goggle display (a head mounted display), a navigation system, an audio reproducing device (e.g., a car audio or an audio component set), a laptop computer, an image reproducing device provided with a recording medium (typically, a device for reproducing a recording medium such as a digital versatile disc (DVD) and having a display for displaying the reproduced image), and the like can be given. FIGS. **19**A to **19**C show specific examples of these electronic devices.

FIG. **19**A shows a mobile phone, which includes a main body **2101**, a display portion **2102**, an audio input portion **2103**, an audio output portion **2104**, and operation keys **2105**. By using the display device of the present invention for the display portion **2102**, a mobile phone in which power consumption can be suppressed can be obtained.

FIG. **1913** shows a video camera, which includes a main body **2601**, a display portion **2602**, a housing **2603**, an external connection port **2604**, a remote control receiving portion **2605**, an image receiving portion **2606**, a battery **2607**, an audio input portion **2608**, operation keys **2609**, an eyepiece portion **2610**, and the like. By using the display device of the present invention for the display portion **2602**, a video camera in which power consumption can be suppressed can be obtained.

FIG. **19**C shows an image display device, which includes a housing **2401**, a display portion **2402**, a speaker portion **2403**, and the like. By using the display device of the present invention for the display portion **2402**, an image display device in which power consumption can be suppressed can be obtained. Note that the image display device corresponds to all image display devices for displaying images, such as those for personal computers, television broadcast reception, and advertisement display.

As described above, the application range of the present invention is extremely wide and the present invention can be applied to electronic devices in all fields.

Although this embodiment is described with reference to various drawings, the contents (or may be part of the contents) described in each drawing can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in another drawing. Further, even more drawings can be formed by combining each part with another part in the above-described drawings.

Similarly, the contents (or may be part of the contents) described in each drawing of this embodiment can be freely applied to, combined with, or replaced with the contents (or may be part of the contents) described in a drawing in another embodiment mode or embodiment. Further, even more drawings can be formed by combining each part with part of another embodiment mode or embodiment in the drawings of this embodiment.

This embodiment shows an example of an embodied case of the contents (or may be part of the contents) described in other embodiment modes and embodiments, an example of slight transformation thereof, an example of partial modification thereof, an example of improvement thereof, an example of detailed description thereof, an application example thereof, an example of related part thereof, or the like. Therefore, the contents described in other embodiment modes and embodiments can be freely applied to, combined with, or replaced with this embodiment.

This application is based on Japanese Patent Application serial No. 2007-004106 filed with Japan Patent Office on Jan. 12, 2007, the entire contents of which are hereby incorporated by reference.

What is claimed is:

1. A display device comprising:

at least a first memory circuit configured to store lines of data of video signals corresponding to a plurality of frame periods;

a data comparison circuit configured to read the lines of data of the video signals from the first memory circuit, compare the lines of data, and extract groups each including at least two lines of data corresponding to at least two different line periods in which the data of video signals correspond to each other, the at least two different line periods being non-adjacent;

a pixel portion including a plurality of pixels; and

a signal line driver circuit including a sampling circuit and a plurality of latch circuits each connected to the sampling circuit and configured to sequentially output the at least two lines of data of the at least two different line periods, each latch circuit being configured to concurrently hold data of video signals corresponding to one of the groups.

2. The display device according to claim **1**, wherein the data comparison circuit includes:

a counter configured to count a number of the at least two lines of data included in each of the groups.

3. The display device according to claim **1**, wherein the data comparison circuit is configured to control the plurality of latch circuits so that writing of data of the groups is performed only once in second memory circuits included in the display device other than the first memory circuit.

4. The display device according to claim **1**, further comprising a scan line driver circuit configured for selecting the plurality of pixels in each line.

5. The display device according to claim **1**, wherein the display device is incorporated in an electronic device selected from the group consisting of a camera, a computer, an image reproducing device, a goggle-type display, a game machine, projector, and a mobile phone.

6. A display device comprising:

a pixel portion comprising a plurality of pixels arranged in a matrix including lines of pixels;

a driver circuit configured to drive the pixel portion;

a sampling circuit and a plurality of latch circuits each connected to the sampling circuit, the sampling circuit and the plurality of latch circuits being comprised in the driver circuit;

a memory configured to store data of video signals corresponding to line periods included into a plurality of frame periods, each line period corresponding to writing of video data to a line of pixels; and a data comparison circuit configured to compare data corresponding to two non-adjacent lines of pixels, and to control writing and holding of identical data to be written into two non-adjacent lines of pixels in the latch circuits,

wherein the driver circuit is configured to hold the identical data while being input with different pieces of data of video signal corresponding to a line period located between the two non-adjacent line periods and while inputting the different pieces of data to the pixel portion.

7. The display device according to claim **6**, wherein the data comparison circuit is configured to control writing and holding of data in the latch circuits in accordance with a result of the comparison.

8. The display device according to claim **6**, wherein the data comparison circuit is further configured to extract a plurality of line periods in which data of video signals correspond to each other.

9. The display device according to claim **8**,

wherein the data comparison circuit is further configured to:

write the corresponding data of video signals into the plurality of latch circuits; and

make the plurality of latch circuit hold the corresponding data of video signals until the corresponding data of video signals have been input to lines of pixels corresponding to the extracted plurality of line periods.

10. The display device according to claim **9**, wherein the corresponding data of video signals are hold in a same latch circuit while a plurality of lines of pixels are input with the corresponding data of video signals.

11. The display device according to claim **6**, further comprising a scan line driver circuit configured for selecting the plurality of pixels in each line.

12. The display device according to claim **6**, wherein the display device is configured so that data identical in the two lines of pixel can be hold in one of the latch circuits while being inputted in each of the two lines of pixels.

13. The display device according to claim **6**, wherein the display device is incorporated in an electronic device selected from the group consisting of a camera, a computer, an image reproducing device, a goggle-type display, a game machine, projector, and a mobile phone.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 9,171,492 B2
APPLICATION NO. : 14/170693
DATED : October 27, 2015
INVENTOR(S) : Yasunori Yoshida

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Specification

Column 4, line 51, replace "transitivity" with --transmittivity--;

Column 28, line 23, before "to" replace "RS_4" with --RS_1--;

Column 32, line 39, after "substrates" replace "." with --,--;

Column 39, line 27, after "which" replace "ran" with --can--;

Column 44, line 10, after "FIG." replace "2313" with --23B--;

Column 46, line 38, after "Thus" replace ";" with --,--;

Column 49, line 64, after "FIG." replace "2913" with --29B--;

Column 50, line 10, after "mounted" replace "an" with --on--;

Column 51, line 51, after "R," insert --G,--;

Column 55, line 11, after "FIG." replace "3313" with --33B--;

Column 62, line 7, after "capacitor" replace "40301" with --40303--;

Column 77, line 48, after "Ta2," replace "Ta1," with --Ta3,--;

Column 84, line 57, after "pixel" replace "d" with --called--;

Column 93, line 66, after "LDD" replace "(Loft)" with --(Loff)--;

Column 99, line 62, after "film)" insert --.--;

Column 104, line 12, after "nitride" replace "(MN)," with --(AlN),--;

Column 109, line 52, after "and" replace "7113" with --71B--;

Column 110, line 3, after "FIG." replace "7113" with --71B--;

Column 118, line 52, after "signal" replace "," with --.--;

Column 123, line 43, after "of a" replace "minor" with --mirror--;

Column 131, line 10, after "embodiment" replace "," with --.--; and

Column 135, line 35, after "FIG." replace "1913" with --19B--.

Signed and Sealed this
Fifth Day of April, 2016

Michelle K. Lee

Michelle K. Lee
Director of the United States Patent and Trademark Office